EXHIBIT 4

[redacted]

Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 11,016,918

Issued: May 25, 2021

Filed: December 30, 2020

Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta

Title: Flash-DRAM Hybrid Memory Module

Inter Partes Review No. IPR2022-00996

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,016,918

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CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory module comprising:
1.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
1.c	a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
1.d	a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
1.e	a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
1.f	a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
1.g	a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
1.h	a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
1.i	[1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, [2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, [3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.
2	2. The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.

Ref. #	Listing of Challenged Claims
3	3. The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.
4	4. The memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively.
5.a	5. The memory module of claim 1, further comprising:
5.b	a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.
6	6. The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.
7	7. The memory module of claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage.
8.a	8. The memory module of claim 1, the plurality of components further comprising:
8.b	[1] one or more registers coupled to one of the first, second, third and fourth regulated voltages, [2] the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, [3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.
9	9. The memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage.
10.a	The memory module of claim 5, the plurality of components further comprising:
10.b	a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

Ref. #	Listing of Challenged Claims
11	11. The memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.
12.a	12. The memory module of claim 5, the plurality of components further comprising:
12.b	a non-volatile memory; and
12.c	a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.
13	13. The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.
14	14. The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.
15.a	15. The memory module of claim 1, the plurality of components further comprising:
15.b	a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.
16.a	A memory module comprising:
16.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
16.c	first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

Ref. #	Listing of Challenged Claims
16.d	[1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, [2] wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;
16.e	a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and
16.f	a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.
17	17. The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.
18.a	18. The memory module of claim 16, the plurality of components further including:
18.b	a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.
19	19. The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.
20	20. The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.
21.a	21. The memory module of claim 16, the plurality of components further including:

Ref. #	Listing of Challenged Claims
21.b	[1] at least one circuit coupled between the interface and the plurality of SDRAM devices, [2] the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices, [3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.
22.a	22. The memory module of claim 16, the plurality of components further including:
22.b	a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.
23.a	A memory module comprising:
23.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
23.c	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, [3] wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections;
23.d	first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

Ref. #	Listing of Challenged Claims
23.e	a converter circuit configured to provide the fourth regulated voltage,
23.f	wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,
23.g	wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and
23.h	wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.
24.a	24. The memory module of claim 23, further comprising:
24.b	a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.
25.a	25. The memory module of claim 24, the plurality of components further including:
25.b	a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.
26	26. The memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory.
27	27. The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.
28	28. The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.
29	29. The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

Ref. #	Listing of Challenged Claims
30	30. The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

I. PETITIONER'S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd., and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 11,016,918.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00999 (U.S. Patent No. 11,232,054)
- Application No. 17/582,797

The following proceeding is no longer pending:

- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00692 (U.S. Patent No. 8,874,831)

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Lead Counsel is Eliot D. Williams (Reg. No. 50,822), DLSamsungNetlistIPRs@BakerBotts.com, (650) 739-7511, Baker Botts L.L.P., 1001 Page Mill Road, Building One, Suite 200, Palo Alto, CA 94304.

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- Brianna L. Potter (Reg. No. 76,748), DLSamsungNetlistIPRs@BakerBotts.com, (650) 739-7556

The fax number for lead and backup counsel is (650) 739-7611.

D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail to DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-30 of U.S. Patent 11,016,918 ("918 Patent") (EX1001) based on grounds not considered during prosecution.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Standing (§42.104(a))

Petitioner certifies that the 918 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the 918 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-30 of the 918 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	1-3, 8, 14-15, 23	103(a)	Harris + FBDIMM Standards
2	1-30	103(a)	Ground 1 + Amidi
3	1-30	103(a)	Ground 2 + Hajeck
4	1-30	103(a)	Spiers+Amidi
5	1-30	103(a)	Ground 4 + Hajeck

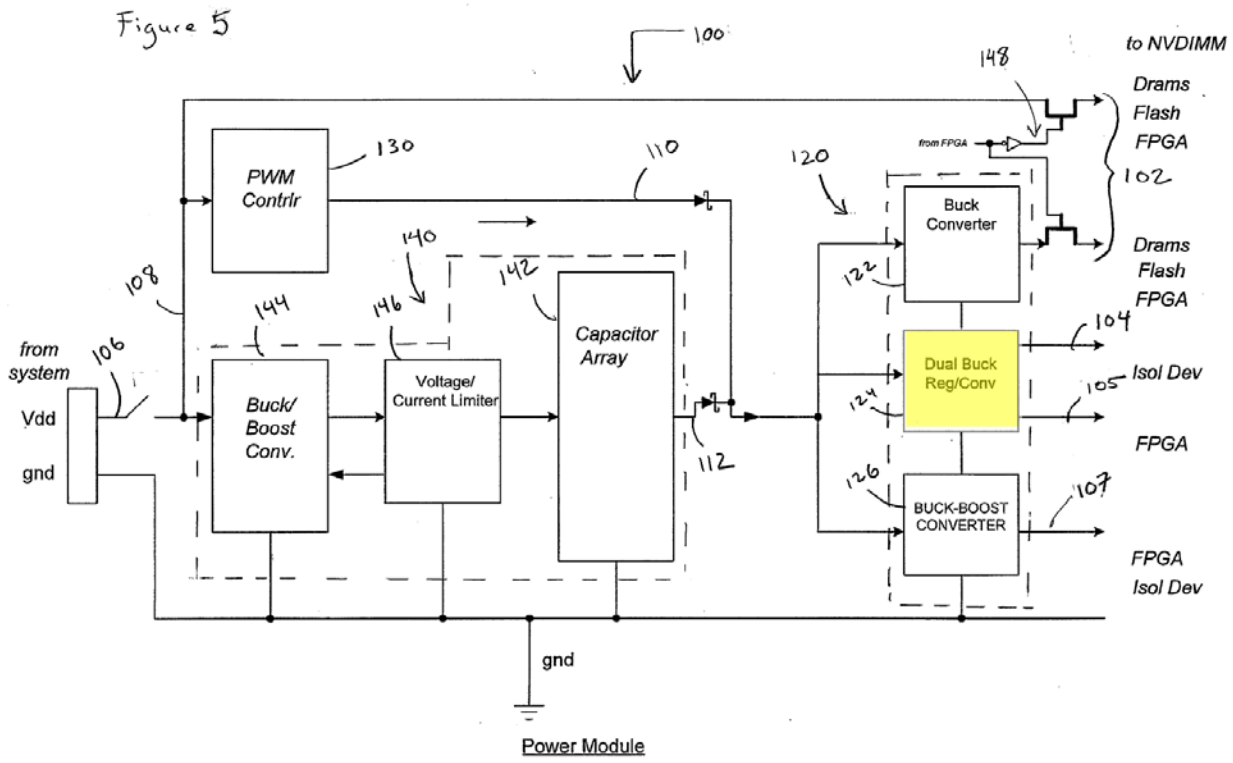
Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above on page vi.

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date of the 918 Patent

All the prior art in the Grounds above predates June 1, 2007, when the earliest provisional application for the 918 Patent was filed, but to the extent it matters, the claims of the 918 Patent do not appear to have support in any application filed before ***June 2, 2008***. EX1003, ¶¶47-66. For example, the three "buck converter" and one "converter circuit" claim limitations (resulting in four regulated voltages) lack support in the earliest provisional, which just discloses a "step-down transformer 84." EX1005, ¶[0017]; EX1003, ¶¶50-58. Furthermore, there is no disclosure of a "dual buck converter" in the earliest provisional, and even the later applications fail to disclose a "dual buck converter" providing a first regulated voltage coupled ***to the SDRAM devices*** as required by several claims. EX1006, pp.19-20, 49 (below);[1] EX1003, ¶¶59-66.

[1] Unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.



B. The 918 Patent

1. Technical Overview

The 918 Patent describes a memory system 1010 that "can be coupled to a host computer system and can include a volatile memory subsystem 1030 [yellow], a non-volatile memory subsystem 1040 [green], and a controller 1062 [red] operatively coupled to the non-volatile memory subsystem 1040," as well as a "second power supply 1080" (blue) comprising either "capacitors" or a "battery" to supply power during a power failure, as shown in Figure 12 (below). EX1001, 21:16-20, 26:8-43; EX1003, ¶¶68-81.

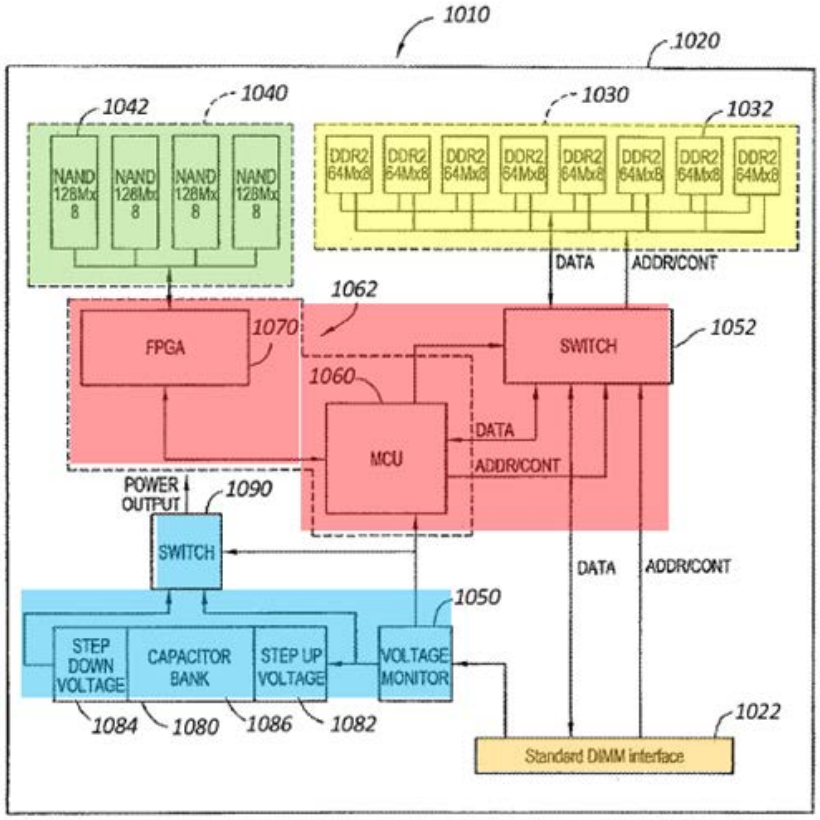


FIG. 12

In the event of a power failure detected by voltage monitor 1050, "[t]he controller [red] backs up the volatile memory [yellow] using the non-volatile memory [green]." EX1001, 20:21-24, 25:8-27.

Figure 16 (below) illustrates a power module 1100 for the memory system above where "sub-block 1122 [below, right] comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter" which output four different voltages (1102=1.8V, 1104=2.5V, 1105=1.2V, 1107=3.3V) to the components of the memory system. EX1001, 27:59-29:64.

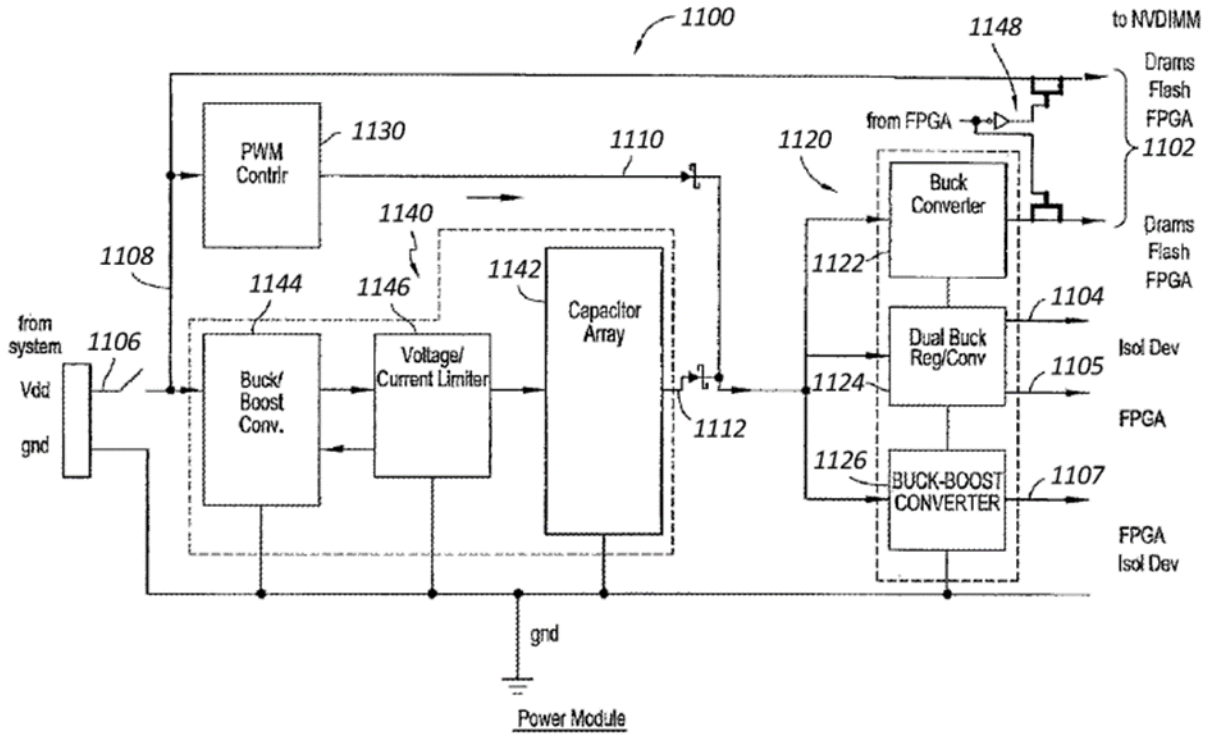


FIG. 16

2. Prosecution History and §325(d)

The 918 Patent was allowed after only one indefiniteness rejection. EX1002, pp.137-43, 157-67. The 918 Patent followed several earlier applications, including two resulting in patents that were later the subject of IPRs: the 833 and 831 patents. EX1003, ¶¶82-127. The claims of the 833 patent are directed to a different invention requiring "different frequencies depending on the mode of operation," as confirmed by an election during prosecution in response to a restriction requirement. EX1007, pp.120-33; EX1003, ¶¶87-89. The IPR against

the 831 patent resulted in a Final Written Decision cancelling all claims. EX1020-21; EX1003, ¶¶99-103.

Advanced Bionics and §325(d) do not support discretionary denial given that the combinations cited by Petitioner were not presented to the Office, and no similar references were evaluated during prosecution. Only one of the references relied on by Petitioner here (Spiers) was marked "considered," but it was buried in an IDS dumping over 100 references into the record, and it was never discussed. EX1002, p.334. Denial under §325(d) is thus unwarranted. *E.g.*, *Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18 at 8-9 (PTAB Aug. 12, 2021).

C. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the field of the 918 Patent in 2008 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. EX1003, ¶67. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller

and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry. *Id.*

D. Construction of Terms Used in the Claims

In related litigation, Patent Owner (Netlist) has interpreted some claim terms broadly for purposes of infringement, EX1071, pp.39-46; EX1073, pp.46-63, even though a narrower interpretation may be more reasonable, but Petitioner contends that no express constructions are needed for this proceeding because the claims are obvious under either interpretation. EX1003, ¶128. It is likewise not necessary to determine whether any terms are governed by §112,¶6, given that for each claim at least one of the prior-art combinations matches the disclosure of the 918 Patent, as discussed below.

V. OVERVIEW OF THE PRIOR ART

A. Harris (EX1023)

U.S. Patent Publication No. 2006/0174140 ("Harris") was published August 3, 2006, and is prior art under §102(a). EX1023. Harris discloses an on-board voltage regulator (102) to convert an externally supplied voltage (104) to appropriate local voltage levels, such as "0.5V to 3.5V," for a wide variety of memory modules (100A), including "fully buffered DIMMs (FBDs)" standardized by JEDEC, comprising "known and heretofore unknown" types of DRAM memory devices (110-1 to 110-N), including those compatible with the DDR2, DDR3, and DDR4 JEDEC standards. *Id.*, Abstract, ¶¶[0009-13], Fig.1A (below); EX1003, ¶¶129-130.

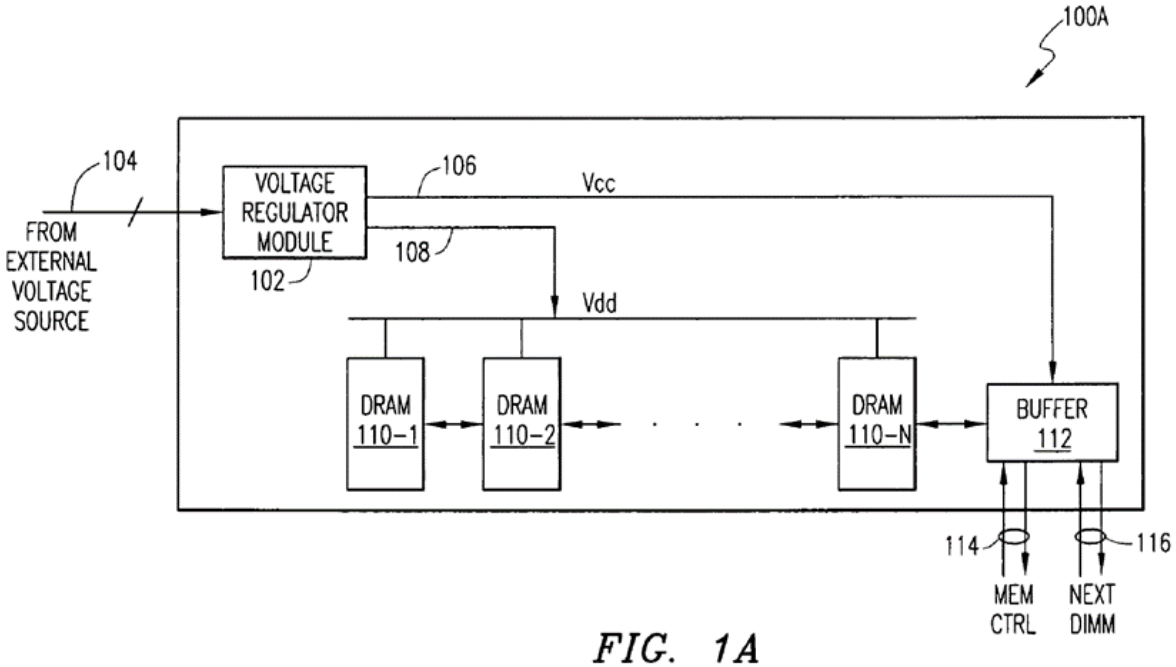


FIG. 1A

B. FBDIMM Standards (EX1027-28)

In March 2007, JEDEC published standards for Fully Buffered DIMM (FBDIMM) memory modules (compatible with Harris, above), including the related "JESD82-20" (EX1027) and "JESD205" (EX1028) standards (collectively, "FBDIMM Standards"). *See* EX1029; EX1003, ¶¶134-136. The FBDIMM Standards are prior art under §102(a).

The FBDIMM Standards specify voltages for components on the memory module, including:

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

EX1028, p.9. With respect to the "AMB buffer" on the memory module, the specified voltages include:

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

EX1027, p.83.

C. Amidi (EX1024)

U.S. Patent No. 7,724,604 ("Amidi"), filed October 25, 2006, is prior art under at least §102(e). EX1024. Amidi teaches monitoring the input voltage to a memory module so that in the event of a power fault, a battery can be used to supply the needed voltages to ensure "a stable power supply even in the face of disruptions." *Id.*, 4:14-22, 8:23-36, Fig.5 (below), Fig.14; EX1003, ¶131-132.

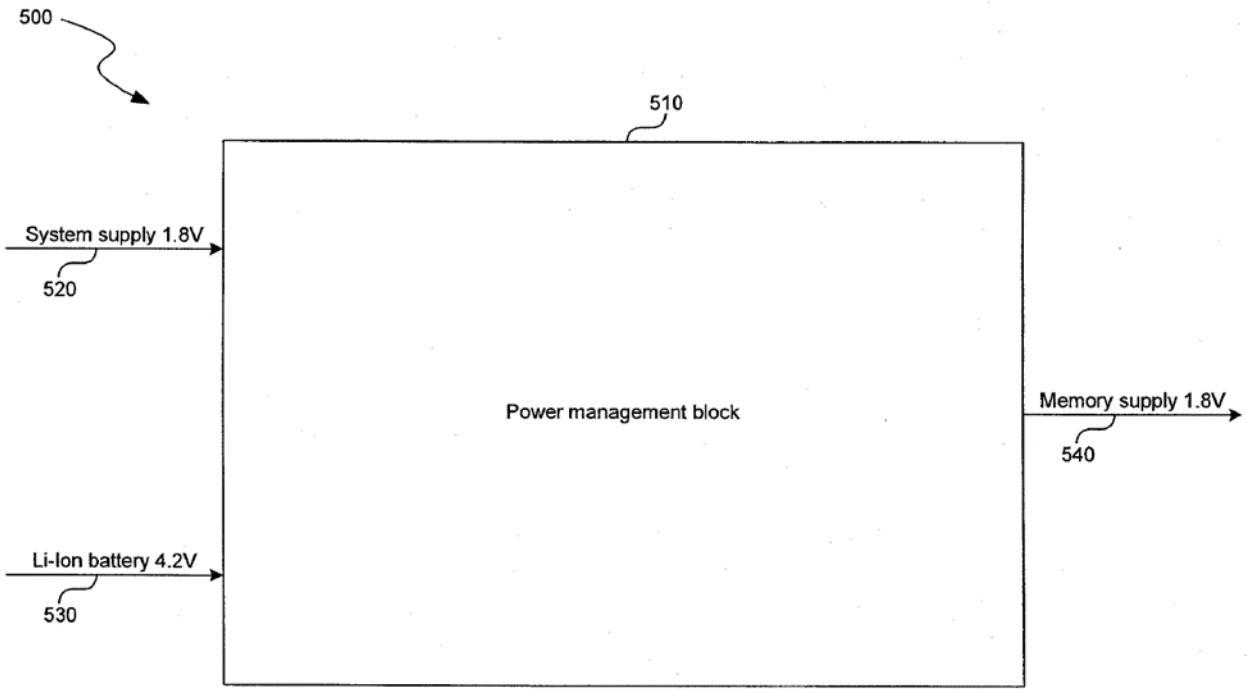


FIG. 5

D. Hajeck (EX1038)

U.S. Patent No. 6,856,556 ("Hajeck"), issued February 15, 2005, is prior art under §102(b). EX1038. Hajeck teaches a voltage detection circuit (48, red) to detect "anomalies" by monitoring the power input to a memory subsystem, including those with volatile and non-volatile memory. *Id.*, Abstract, 3:30-:39,

4:62-65, Fig.1 (below). Such anomalies include undervoltage, *see id*., 3:34-37, and overvoltage, *see id*., 3:37-39. EX1003, ¶137.

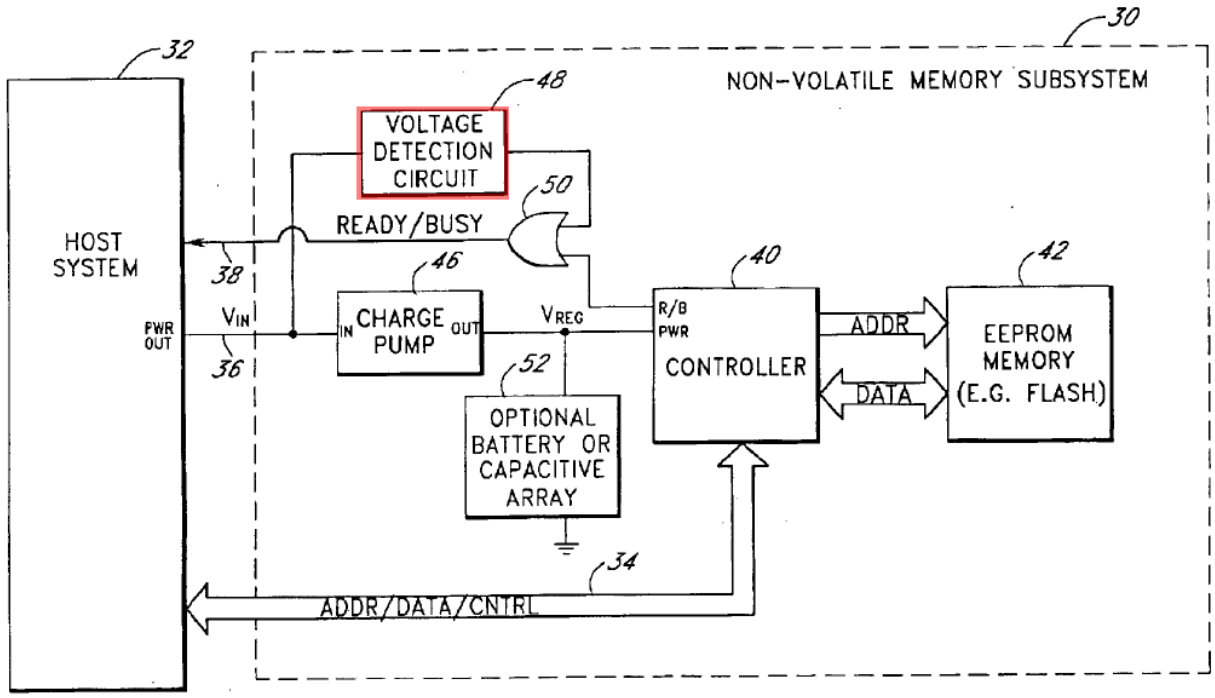


FIG. 1

E. Spiers (EX1025)

U.S. Patent Publication No. 2006/0080515 ("Spiers"), published April 13, 2006, is prior art under §102(b). EX1025. Spiers discloses a memory module (backup device 144) with both volatile (SDRAM) memory (190 and 218, yellow) and non-volatile (NAND flash) memory (194, green), as well as a temporary backup power supply (including capacitors 176, blue) and a processor (198, red)

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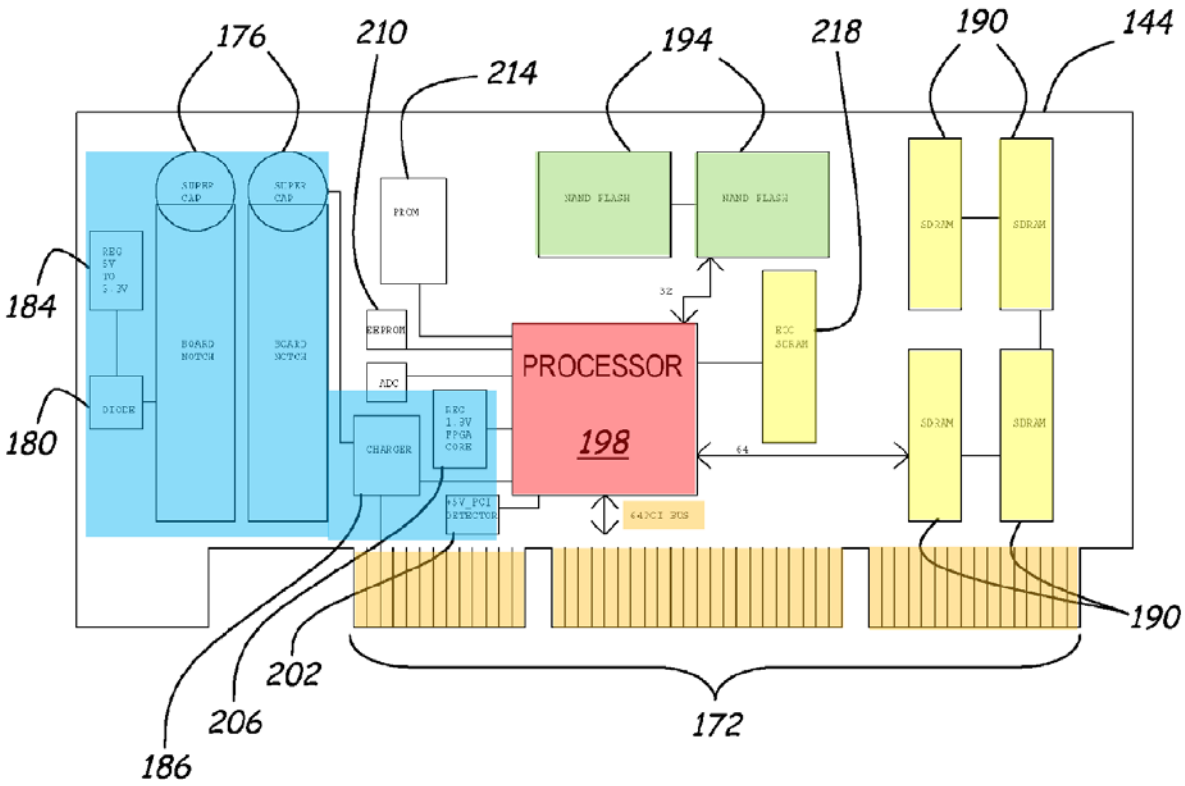
for "moving data from the volatile memory to the non-volatile memory" in the event of a power failure. *Id.*, ¶¶[0037-38], Fig.5 (below); EX1003, ¶133.



VI. ARGUMENT

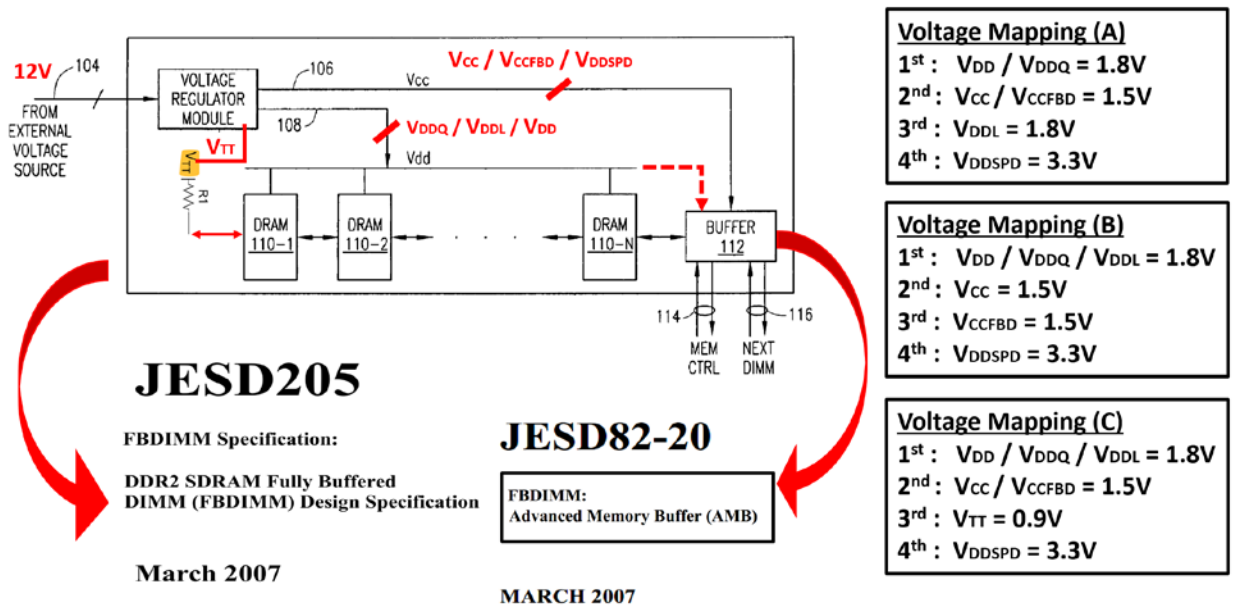
A. Ground 1

Ground 1 renders obvious claims 1-3, 8, 14-15, and 23.

1. Ground 1 combination: Harris (EX1023) + FBDIMM Standards (EX1027-28)

Ground 1 combines Harris with the FBDIMM Standards as follows:

Ground 1: Harris with JEDEC's FBDIMM Standards



EX1003, ¶¶157-169. As explained below, the FBDIMM Standards specify particular voltages, and an embodiment of Harris's Voltage Regulator Module (upper left) can supply those voltages to various components on the memory module.

Harris recognized that "[a]s the performance of the DRAM technology goes up, and timing margins shrink, it is becoming increasingly more difficult for the ***system board*** [power] sources to provide tightly regulated power for the DRAM cores as well as input/output (I/O) interface buffers. Furthermore, each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, 1.8V, 1.5V and beyond), thereby making it difficult to mix memory technologies on a system board...." EX1023, ¶[0002].

Thus, Harris proposes "an ***on-board*** voltage regulator module to generate appropriate local voltage levels." *Id.*, ¶[0003].

A POSITA would have been motivated to combine Harris with the FBDIMM Standards, and had a reasonable expectation of success in doing so, because Harris expressly states that Figure 1A (above) is a "fully buffered DIMM" (i.e., FBDIMM or FBD), EX1023, ¶¶[0009-13], which a POSITA would have known refers to a particular type of memory module standardized by JEDEC's FBDIMM Standards, *id.*, ¶[0013]; EX1003, ¶¶158-165. Thus, a POSITA would naturally look to the FBDIMM Standards for more details about the "fully buffered DIMM" that Harris describes as compatible with his "at least one on-board voltage regulator module (VRM)." *Id.*; EX1023, ¶[0010].

As summarized in the annotated figure above, the FBDIMM Standards specify particular voltages for various components on an FBDIMM, including those below, and thus a POSITA would have been motivated to implement Harris's Voltage Regulator Module (above left) to supply at least the voltages below. EX1003, ¶¶166-169.

- 1.5V for **V_{CC}** and **V_{CCFBD}** to the "AMB" Buffer (112 above).
- 3.3V for **V_{DDSPD}** to the Buffer and the SPD ("Serial Presence Detect," EX1028, p.105) (not shown above).
- 1.8V for **V_{DDQ}**/**V_{DD}** to the Buffer.

- 1.8V for **V_{DDQ}**, **V_{DDL}**, and **V_{DD}** to the "DDR2" DRAM (110-1 to 110-N above).
- 0.9V for **V_{TT}** to the resistors, DRAM, and Buffer.

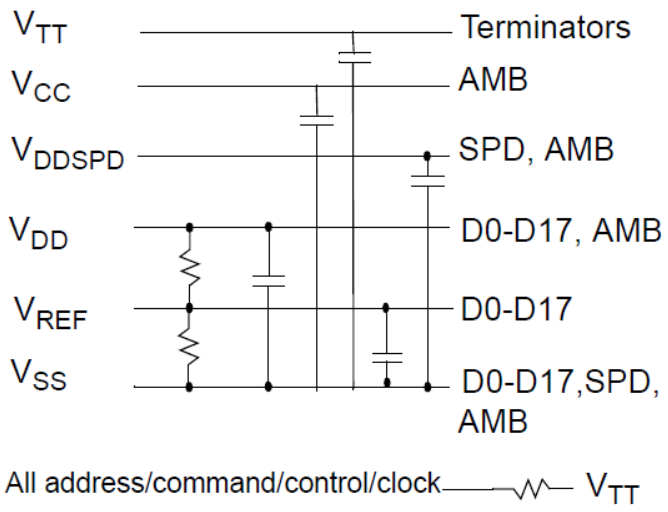
See EX1023, ¶¶[0002-3, 9-10, 17], Figs.1A, 3; EX1028, p.9 (below); *id.*, pp.11-16, 17-20 (V_{DDL}), 30-33, 68; EX1026, pp.6-7 (V_{DDL}, V_{DD}).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

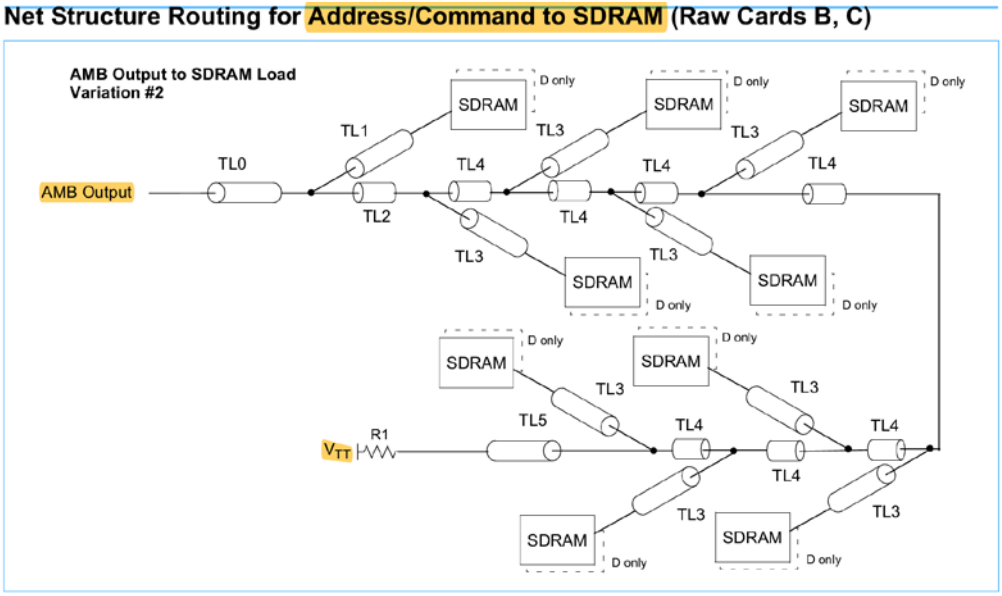
See also EX1027, p.83 (below, for the AMB Buffer); *id.* pp.31-32, 44, 78, 82-83; EX1023, ¶[0017], Fig.3 (V_{DDSPD}).

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

See also, e.g., EX1028, p.15:



Id., p.68:



In the annotated figure for Ground 1 above (p.15), Voltage Mappings "A" to "C" (on the right) are simply different ways to apply the arbitrary labels "1st" through "4th" to the voltages shown in red in the annotated figure. EX1003, ¶¶167-169.

Below, Ground 1A refers to Ground 1 above with Voltage Mapping "A," while Grounds 1B and 1C refer to Ground 1 above with Voltage Mappings "B" and "C," respectively. *Id.*

2. Independent Claim 1

a) [1.a] Preamble

To the extent the preamble is limiting, Grounds 1A-1C teach "*[a] memory module* [e.g., Harris's "memory module 100A" in Fig.1A, and 306 (below)] *comprising.*" EX1023, ¶¶[0009, 17, 20], Figs.1A, 3; EX1003, ¶¶216-222.

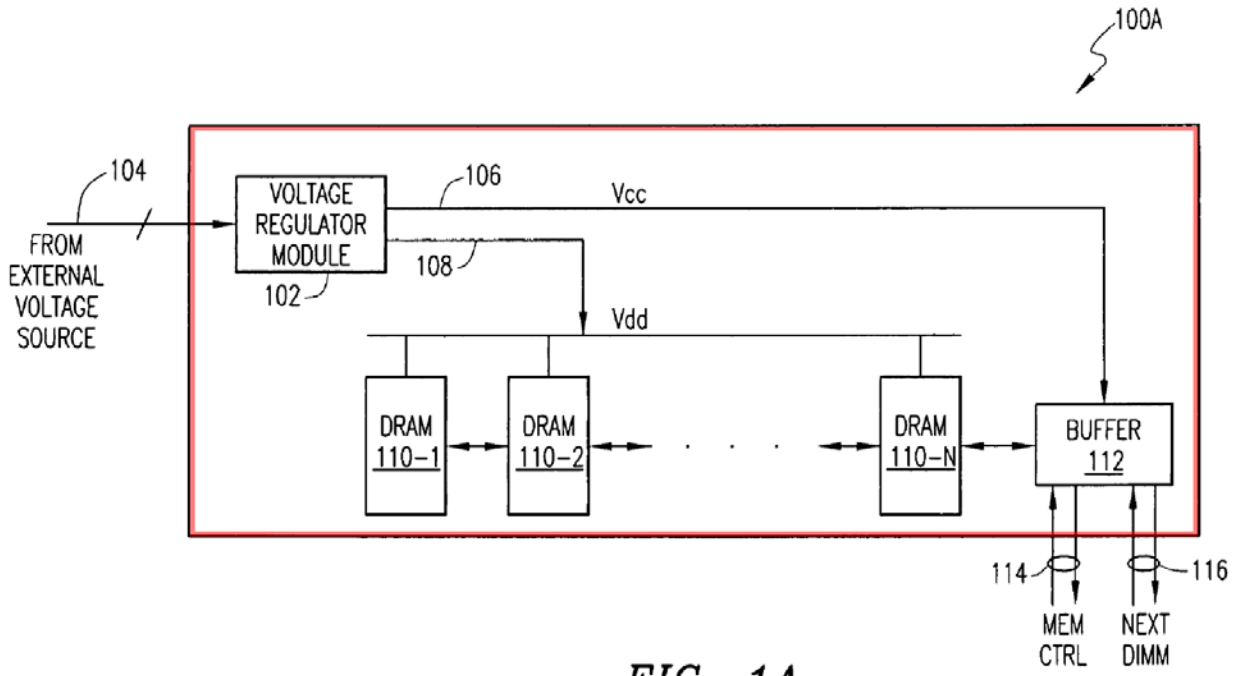


FIG. 1A

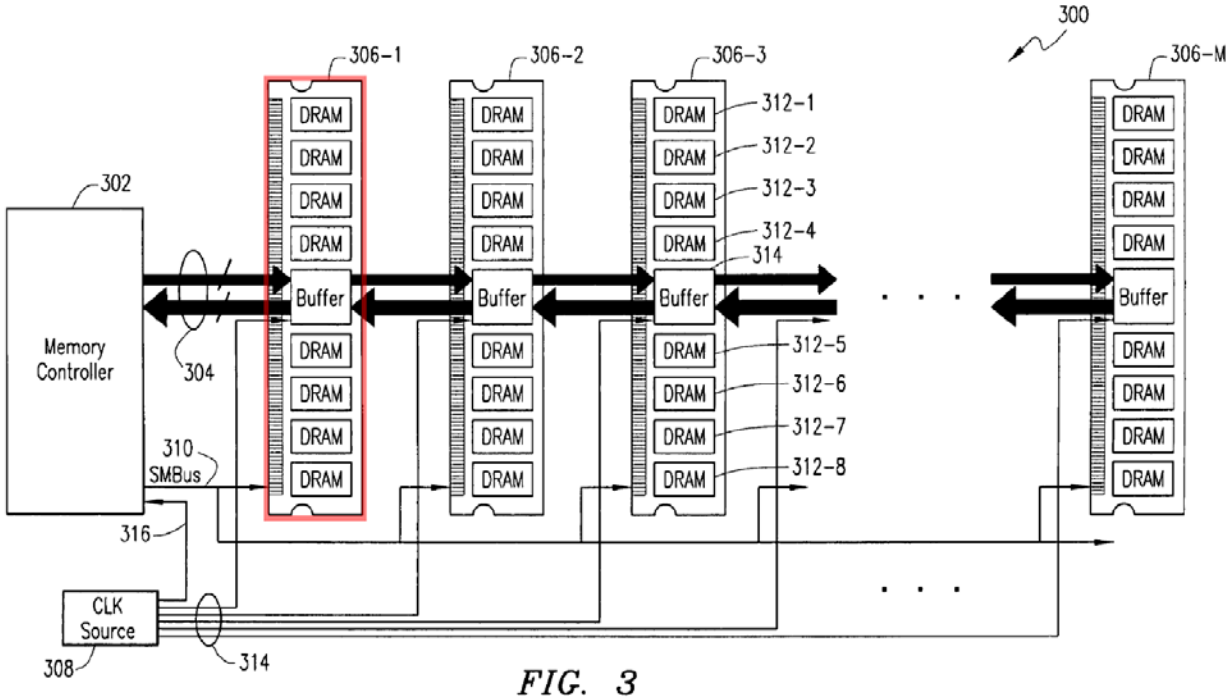
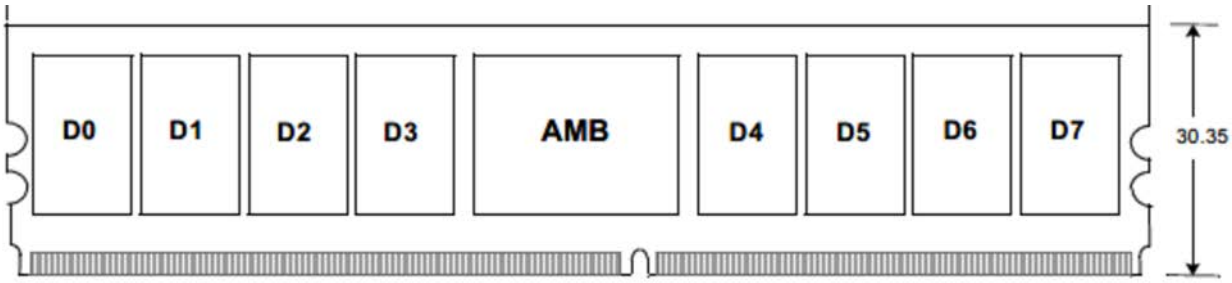


FIG. 3

A POSITA would have recognized the FBDIMM "*memory module[s]*" disclosed by Harris (above) are similar to the "*memory module[s]*" disclosed in JEDEC's FBDIMM Standards (e.g., below):



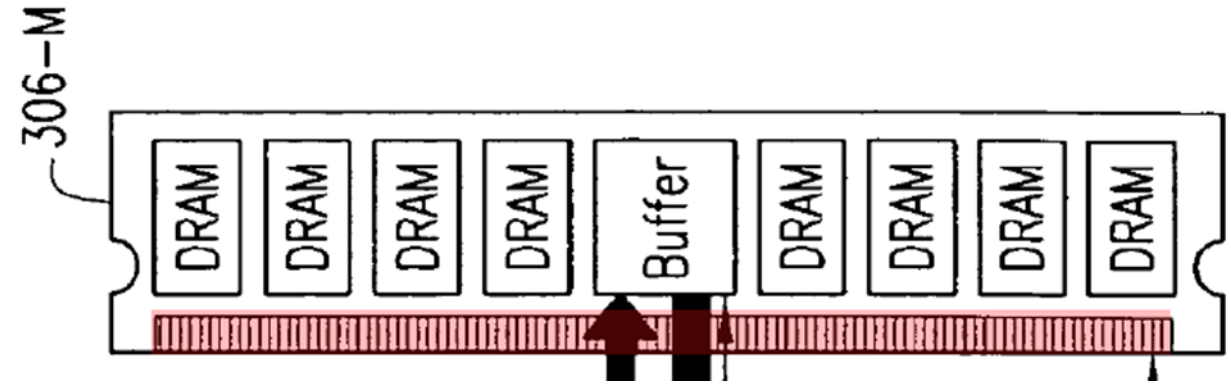
EX1028, p.38; EX1003, ¶221.

b) [1.b] Printed Circuit Board (PCB)

Grounds 1A-1C teach "*a printed circuit board (PCB),*" as shown above for [1.a]. *See also* EX1023, ¶[0013] ("printed circuit board"), ¶[0009] ("memory

board"), Figs.1A, 3; EX1028, pp.10 ("PCBs are called … 'raw cards'"), 38, 84; EX1003, ¶¶223-225.

Grounds 1A-1C teach the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*" (sometimes called "pins") as shown above for [1.a] and reprinted below from Harris's Figure 3. EX1023, ¶¶[0002, 12-13, 19], Figs. 3-4; EX1028, pp.38, 84; EX1003, ¶¶226-227.



Grounds 1A-1C teach the edge connections in Harris, consistent with JEDEC's FBDIMM Standards, are "*configured to couple power, data, address and control signals between the memory module and the host system*":

- "*power*": EX1023, ¶[0012] ("power"/"+12V" "pins"); *id.*, ¶¶[0010, 19] & Fig.1A (104, below).

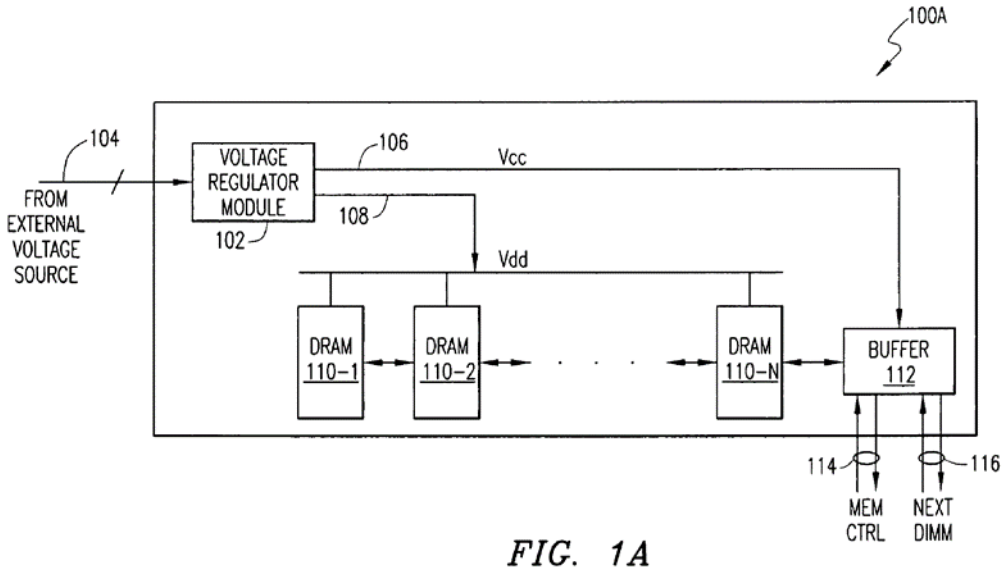
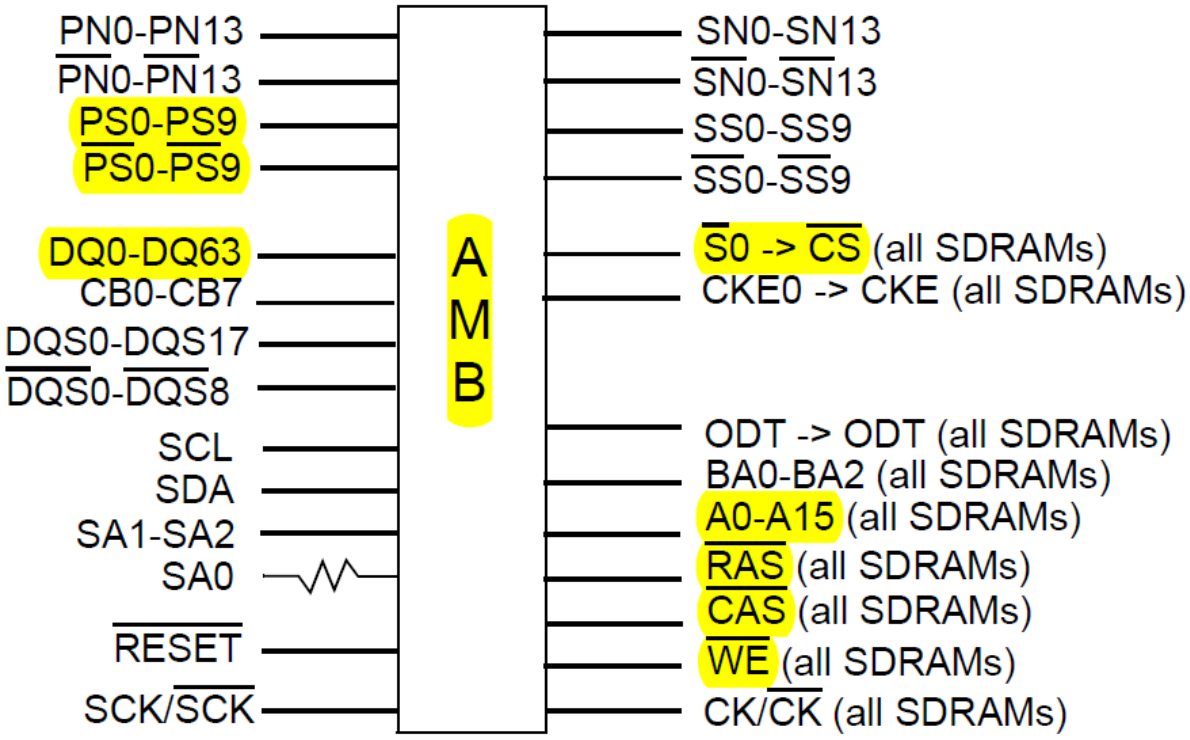


FIG. 1A

Furthermore, as shown in Figure 1A above, Buffer 112 (called "AMB" in the FBDIMM Standards) receives via 114 and transmits to DRAMs 110-1 to 110-N the following signals (as shown below and consistent with JEDEC standards):

- "*data*": e.g., DQ0-DQ63 (below); EX1023, ¶[0009] ("buffer/logic component 112 is provided for buffering command/***address*** (C/A) space as well as ***data*** space at least for a portion of the memory devices 110-1 through 110-N")
- "*address*": e.g., A0-A15 (below); *id.* ("***address***")
- "*control*": e.g., RAS, CAS, WE, CS (below); *id.* & Fig.1A (114, "CTRL"). These "*control*" signals together can form a "command." *See, e.g.*, EX1028, p.29 ("Part of command"); EX1026, pp. 6 ("RAS, CAS and WE (along with CS) define the command"), 46-47, 52.

See also EX1023, ¶¶[0009-12, 17, 19], Figs.1A, 3; EX1028, pp.11, 13 (below), 29; EX1027, pp.1 (AMB "[a]cts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM"), 3-4 (below, "The southbound input link is 10 lanes wide and carries commands and write data from the host….The northbound input link is 13 to 14 lanes wide and carries read return data…back towards the host… There are two copies of address and command signals [output from the AMB to the SDRAMs] to support DIMM routing and electrical requirements."), 7 ("Southbound: The direction of signals running from the host controller toward the DIMMs."), 81-82; EX1026, pp. 6, 46-47, 52; EX1003, ¶¶228-231.



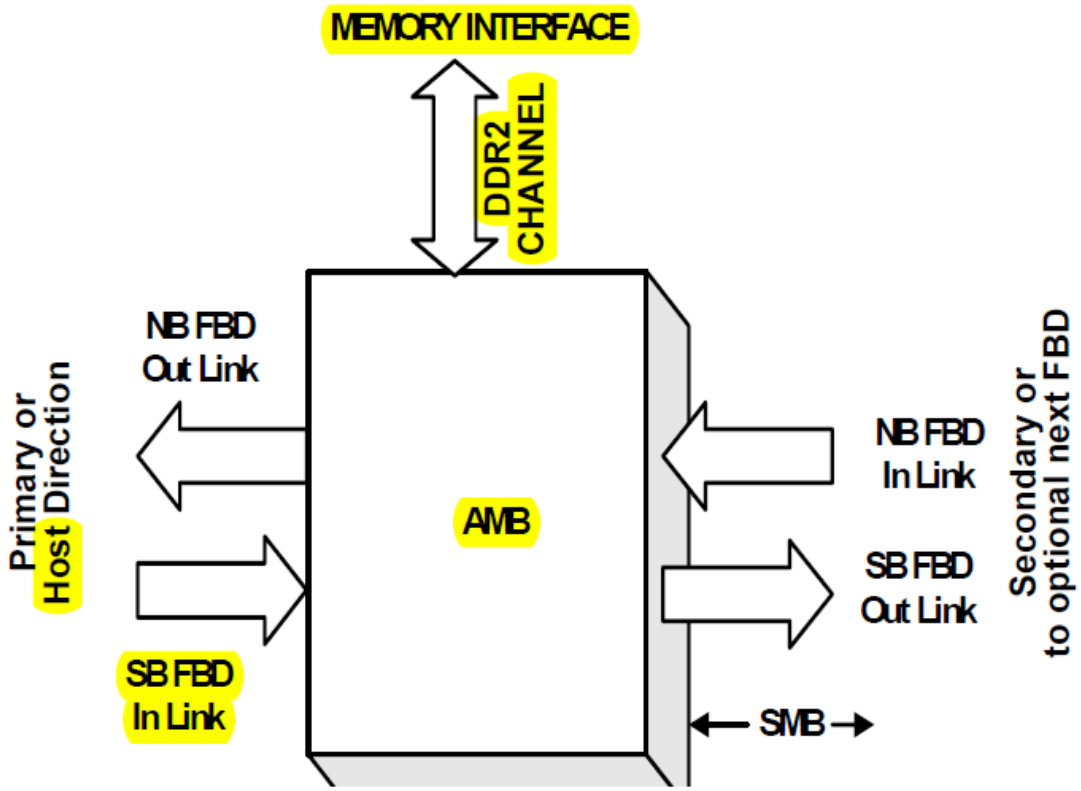


Figure 1.2 — Advanced Memory Buffer Interfaces

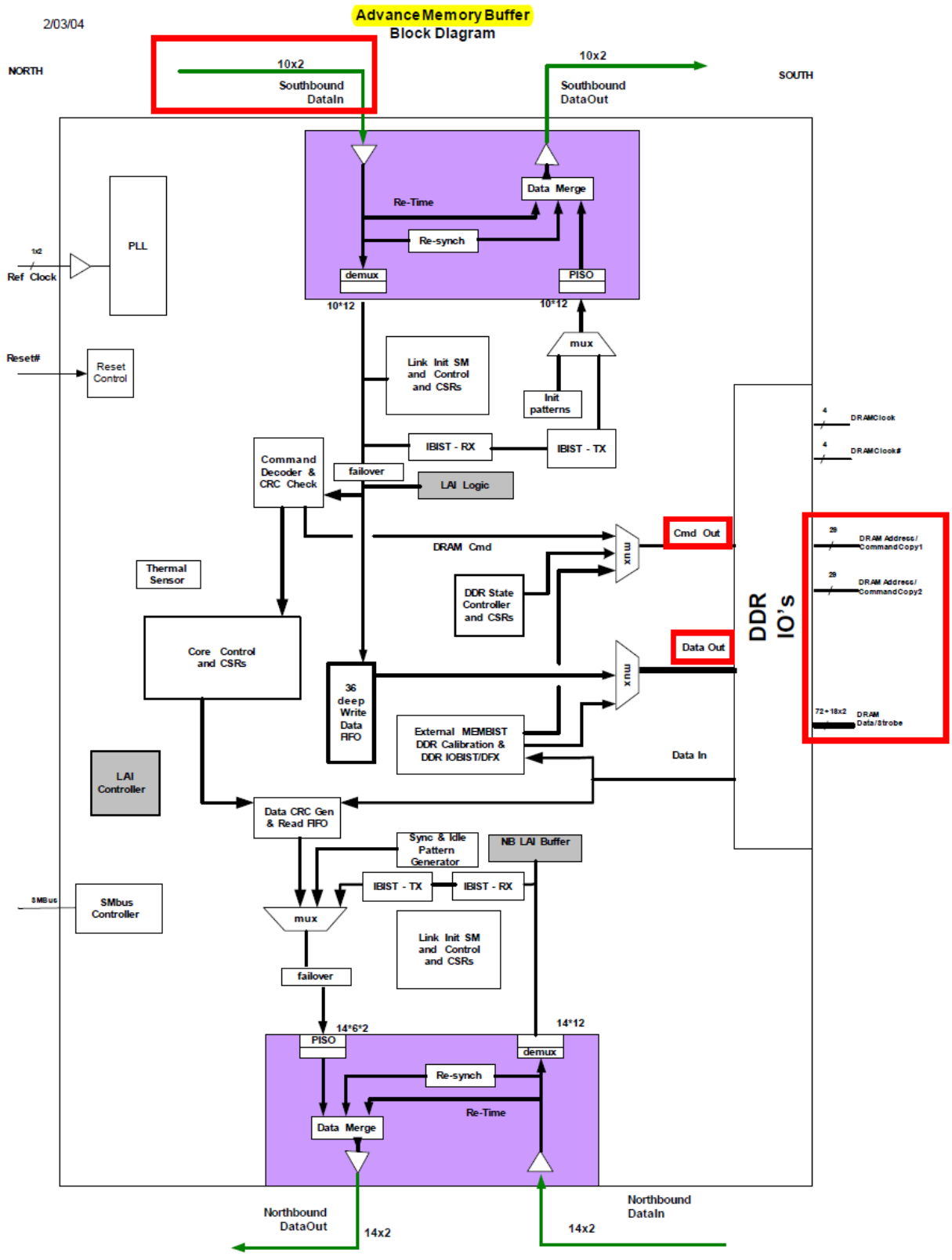
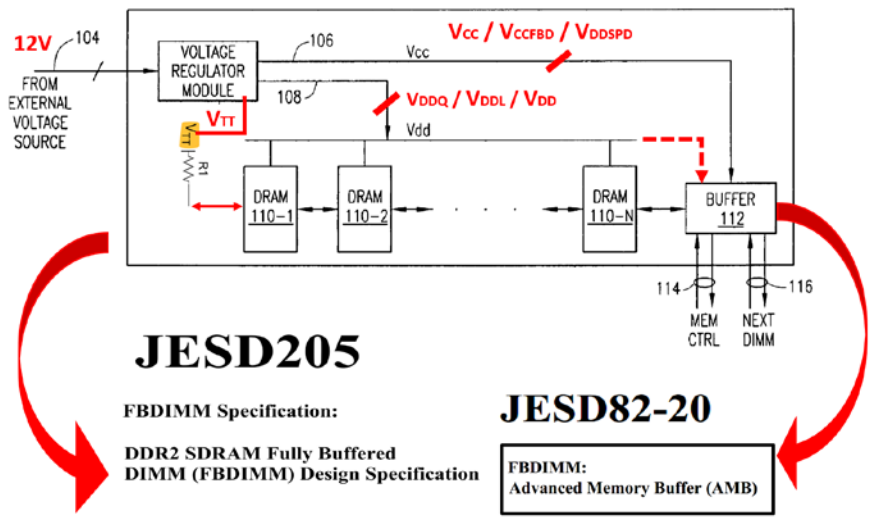


Figure 1.1 — Advanced Memory Buffer Block Diagram

c) [1.c] to [1.f] First to Fourth Regulated Voltages

Grounds 1A-1C teach "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude* ["1st"/"*first*" below]*; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude* ["2nd"/"*second*" below]*; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude* ["3rd"/"*third*" below]*; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude* ["4th"/"*fourth*" below]," as shown in Voltage Mappings A to C below:

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

See supra pp.14-19; EX1003, ¶¶232-243, 250-257, 262-276, 281-287.

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V	V_{DD}, V_{DDQ}, or V_{DDL} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V
"*fourth*":	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V	V_{DDSPD}=3.3V

Id.

As shown above, Grounds 1A-1B have two "*voltage amplitude[s]*" that are the same, consistent with Netlist's broad interpretation of the claim, EX1071, p.43; EX1073, pp.49-53, while Ground 1C does not, consistent with a narrower interpretation.

Furthermore, Harris discloses a range of voltages — "from about 0.5V to 3.5V or more," EX1023, ¶[0009] — as do the FBDIMM Standards, and thus any combination of "*first*" to "*fourth*" voltages in that range would have been obvious: "Where a prior art patent discloses a range of values, showing a claimed value falls within that range meets a party's burden of establishing the narrower claim would have been obvious where there is no reason to think the result would be unpredictable." *Gen. Hosp. Corp. v. Sienna Biopharms., Inc.*, 888 F.3d 1368, 1373 (Fed. Cir. 2018); *see also, e.g.*, *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d

1317, 1320-23 (Fed. Cir. 2004) (claim to three grips obvious in light of prior art teaching one, two, and four grips).

Harris teaches that the voltages above would be "*regulated*": Harris identifies "tightly ***regulated*** power" on the memory module as a problem to be solved, and proposes "at least one ***on-board*** voltage ***regulator***" that is "capable of generating ***tightly-controlled*** voltage levels" as the solution. EX1023, ¶¶[0002-3, 0009-11]; EX1003, ¶234.

Harris also teaches using "*[buck] converter[s]*" to provide the four[2] regulated voltages above. EX1003, ¶¶236-237, 252, 264, 286. Harris discloses "replacing [the prior-art] power supply interface pins with as few as six +12V pins (from an external voltage source)" and then using "a ***high-frequency switching voltage converter*** capable of generating tightly-controlled voltage levels" to provide each needed on-board regulated voltage. EX1023, ¶¶[0012, 0010]. A "buck converter" was a conventional device for implementing such a "***voltage-reducing switching converter***." EX1030, 2:41-43. Furthermore, it would have

[2] The claim language does not expressly state that the "*fourth*" "*converter*" must be a "***buck***" converter, but as explained above, using a buck converter would have been an obvious way to implement the "*fourth*" "*converter*," EX1003, ¶286, regardless of whether the claim is interpreted more broadly than that.

been obvious to a POSITA to use a "*buck converter*" to convert the higher input voltage (e.g., 12V) to the lower output voltage (e.g., 3.5V or less), and there would have been a reasonable expectation of success, given that buck converters were well-known "switching" devices commonly used to step down the voltage between its input and output, as had long been taught in textbooks. EX1003, ¶¶146-149, 236-237; EX1058 (Lenk textbook from 1995), pp.3 ("Figure 1-3 shows three typical MOSFET ***switching-regulator (or -converter)*** circuits, representing the three basic configurations: ***buck***, *boost*, and *buck-boost*…. The ***buck*** circuit is used when the input voltage is always greater than the desired output voltage (and is also known as a *step-down* converter)."), 5 ("1.3 Switching-Regulator Theory"), 12-16 ("1.5.4 Buck or Step-Down"); EX1032 (Mohan textbook from 1995), pp.161 (identifying "Step-down ***(buck) converter***" as a "basic converter topolog[y]."), 164 ("As the name implies, a step-down converter produces a lower average output voltage than the dc input voltage V_d."); EX1024 (Amidi) Fig.6 (showing "DC/DC ***buck***" converter 640 to step down a higher voltage to a lower one); EX1050, 1:21 (identifying buck converters as one of "the most basic building blocks in power electronics").

Further, "buck converters" were well-known as a ***highly-efficient*** way to step down voltages without generating excess heat or requiring large cooling devices, providing a further motivation (beyond Harris's express disclosure above)

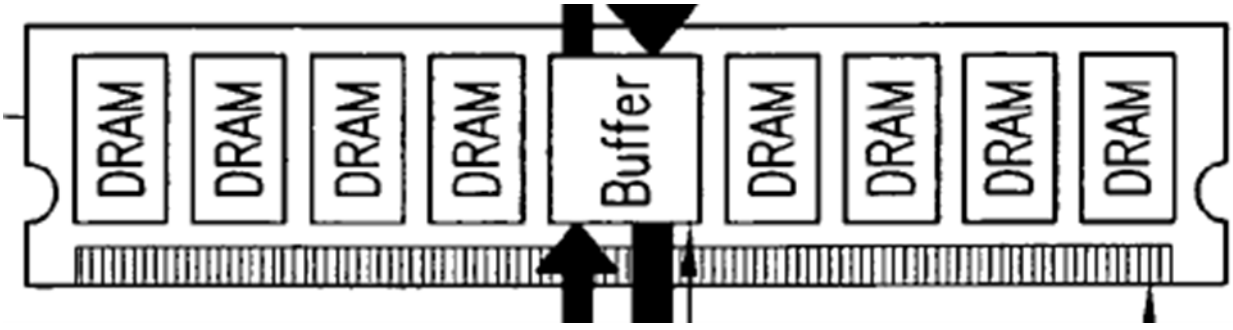
to implement Harris's voltage regulator using "*[buck] converter[s]*." EX1003, ¶237; EX1059, 5:23-30 ("***Switch mode buck converters*** have become popular due to two attractive features: first, they are ***more efficient*** than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, ***they can provide relatively high currents with lower power dissipation on chip than an LDO can***."); EX1058, p.5 (explaining the "***high efficiency*** of switching regulators"); *see also, e.g.*, EX1040, pp.1 ("high efficiency"), 23-24 (Figs.22-25); EX1041, pp. 1, 13 ("high efficiency"); EX1048, p.3; EX1062, p.11; EX1064, ¶[0101].

It would have been obvious to use at least ***four*** converters in Harris given the need for at least ***four*** different voltages in the FBDIMM Standards (e.g., 0.9V, 1.5V, 1.8V, 3.3V), as discussed above (pp. 14-19) and as shown in Voltage Mapping C. Furthermore, with respect to Voltage Mappings A and B (where two of the voltages are the same amplitude, either 1.5V or 1.8V), it also would have been obvious to use ***four*** converters because the two voltages with the same amplitude are ***separate*** voltages in the FBDIMM Standards as discussed above (pp. 14-19). In particular, although V_{DD} and V_{DDQ} and V_{DDL} are all 1.8V, they are expressly identified as separate voltages with separate pins, *see, e.g.*, EX1028, pp.17-20, and JEDEC states that in one implementation they can be turned on and off separately, EX1026, p.9, and that V_{DDL} should use an isolated voltage source, *id.*, pp.2-3, providing a motivation to use separate converters for those voltages so

that they can be controlled separately. EX1003, ¶242; *see also, e.g.*, EX1062, p.13 ("[A] particular standard voltage level may have to be ***independently*** furnished in numerous places …. to improve efficiency … or to meet sequencing requirements…."). Similarly, although V_{CC} and V_{CCFBD} are both 1.5V, they are expressly identified as separate voltages with separate pins, *see, e.g.*, EX1028, pp.30-32, which a POSITA would have understood provides independence for these power supplies to allow improved stability for each supply and flexibility for power management, providing a motivation to use separate converters for those voltages so that they can be controlled separately. EX1003, ¶256.

d) [1.g] A Plurality of Components Coupled to the PCB

Grounds 1A-1C teach "*a plurality of components coupled to the PCB* [e.g., a Buffer and DRAMs (as shown in Harris's Figure 3, below) and an SPD and resistors, as discussed above, pp.14-19], *each component of the plurality of components coupled to one or more regulated voltages of the first second, third and fourth regulated voltages* [as shown above, pp.14-19] *the plurality of components comprising*." EX1003, ¶¶288-290, 293-297.



e) [1.h] A Plurality of SDRAM Devices

Grounds 1A-1C teach "*a plurality of synchronous dynamic random access memory (SDRAM) devices* [e.g., Harris's "Double Data Rate (DDR) dynamic random access memory (DRAM) device[s]" 110-1 to 110-N, *see* EX1023, ¶¶[0009, 11], Figs.1A, 3] *coupled to the first regulated voltage* [e.g., V_{DD}, V_{DDQ}, or V_{DDL}, as shown above, pp.14-19]." EX1003, ¶¶298-303. A POSITA would know that according to the JEDEC standards, "DDR" memory devices are "*synchronous*" DRAM (i.e., SDRAM). *Id.*; EX1028, p.9 ("Double Data Rate ***Synchronous*** DRAM … ***S***DRAM"); EX1045, p.Cover ("(DDR) ***S***DRAM"); EX1026, p.Cover-1 ("DDR2 ***S***DRAM"); EX1046, p.Cover ("DDR3 ***S***DRAM").

f) [1.i.] At least one circuit

(1) [1.i.1] Coupled between edge connections and SDRAM devices and [1.i.2] operable to receive/output address and control signals

Grounds 1A-1C teach "*at least one circuit* [e.g., Harris's "Buffer," which receives data, address, and control signals via 114 across the edge connections, and transmits them to DRAMs 110-1 to 110-N, as discussed in [1.b] above (pp.20-25)] *coupled between a first portion of the plurality of edge connections* [see [1.b]] *and the plurality of SDRAM devices* [see [1.h]], *the at least one circuit* [e.g., Harris's "Buffer"] *operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections* [e.g., via 114 in Fig.1A below, as discussed in [1.b] above (pp.20-25)], *and (ii) output a second plurality of*

address and control signals to the plurality of SDRAM devices [e.g., from Buffer 112 to DRAM 110-1 to 110-N in Fig.1A below, as discussed in [1.b] above (pp.20-25)]." EX1003, ¶¶304-317.

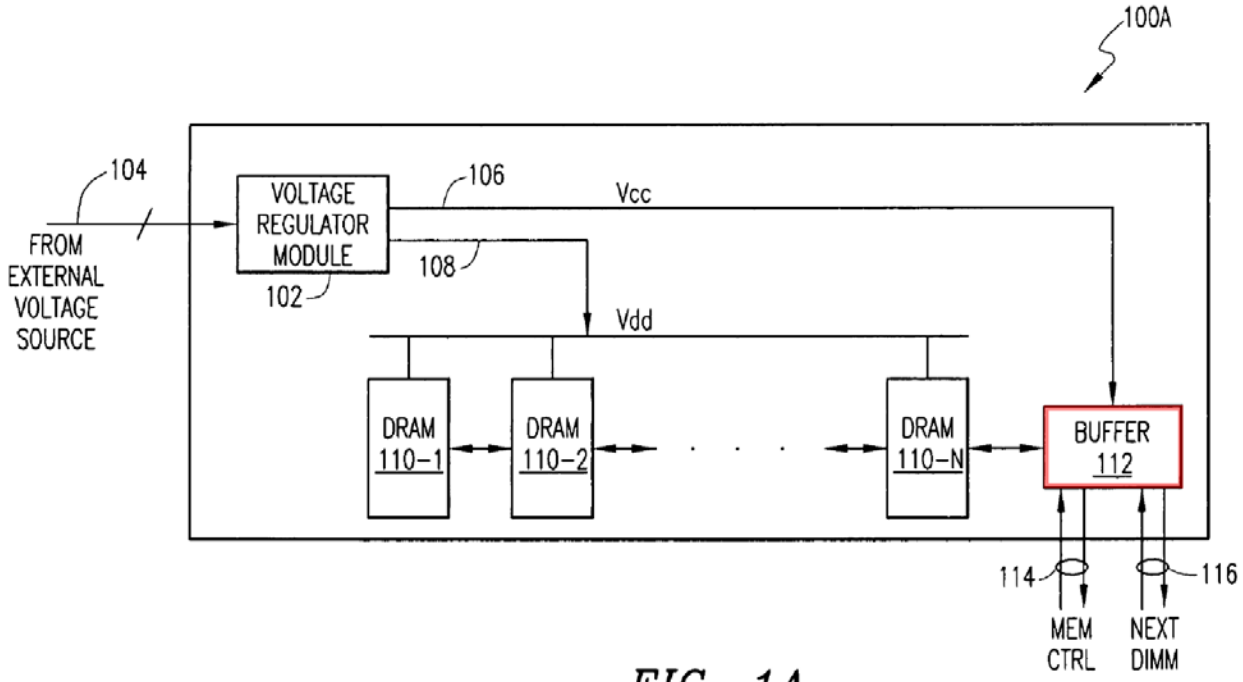


FIG. 1A

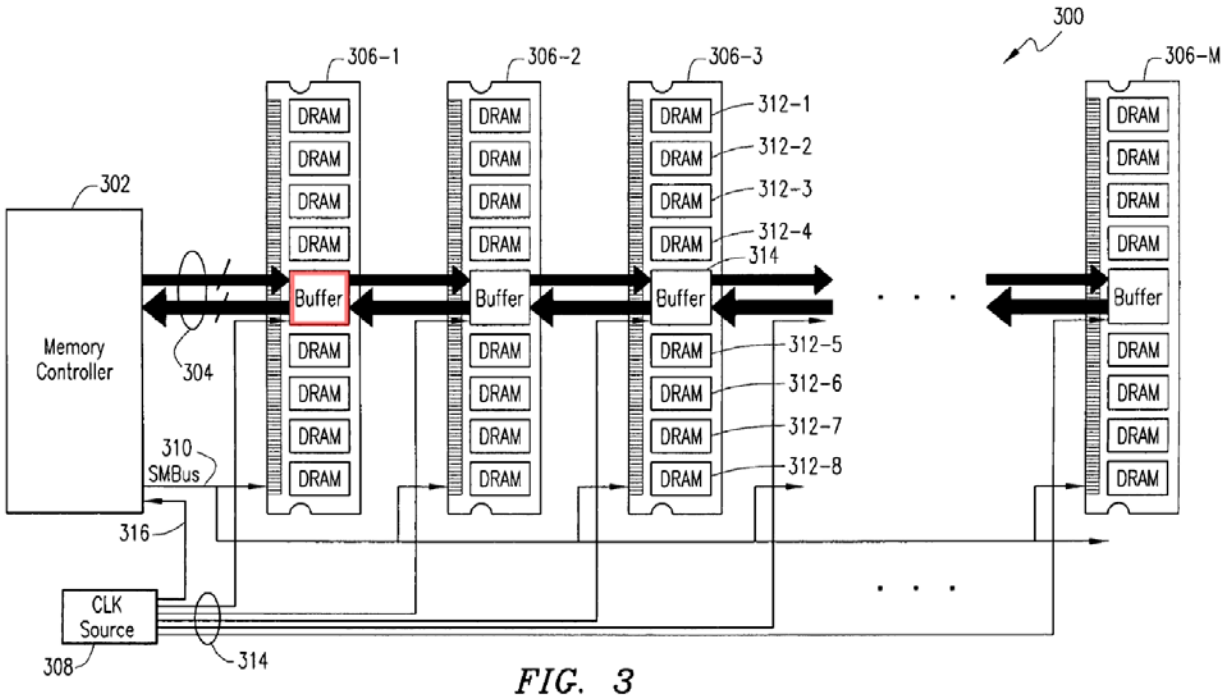
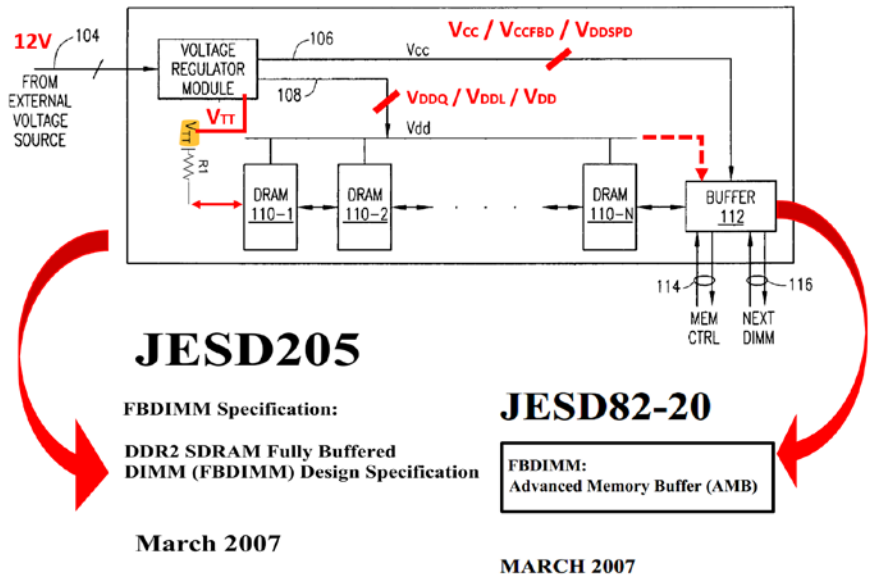


FIG. 3

(2) [1.i.3] Coupled to both the second and fourth regulated voltage

Grounds 1A-1C teach "*the at least one circuit* [e.g., Harris's "Buffer" from [1.i.1]] *coupled to both the second regulated voltage* [e.g., V_{CC} or V_{CCFBD} =1.5V] *and the fourth regulated voltage* [e.g., V_{DDSPD} =3.3V]," as shown below and discussed above (pp.14-19, 27). EX1003, ¶¶318-323.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

(3) [1.i.4] Wherein the second and fourth regulated voltage amplitudes are different

Grounds 1A-1C teach "*wherein one of the second and fourth voltage amplitudes* [e.g., 1.5V] *is less than a second one of the second and fourth voltage amplitudes* [e.g., 3.3V]," as shown above (pp.14-19, 27). EX1003, ¶¶324-327.

3. Claim 2

Grounds 1A-1C teach "*claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.*" EX1003, ¶¶328-347. The 918 Patent illustrates a "*dual buck converter*" as simply having ***two*** outputted voltages:

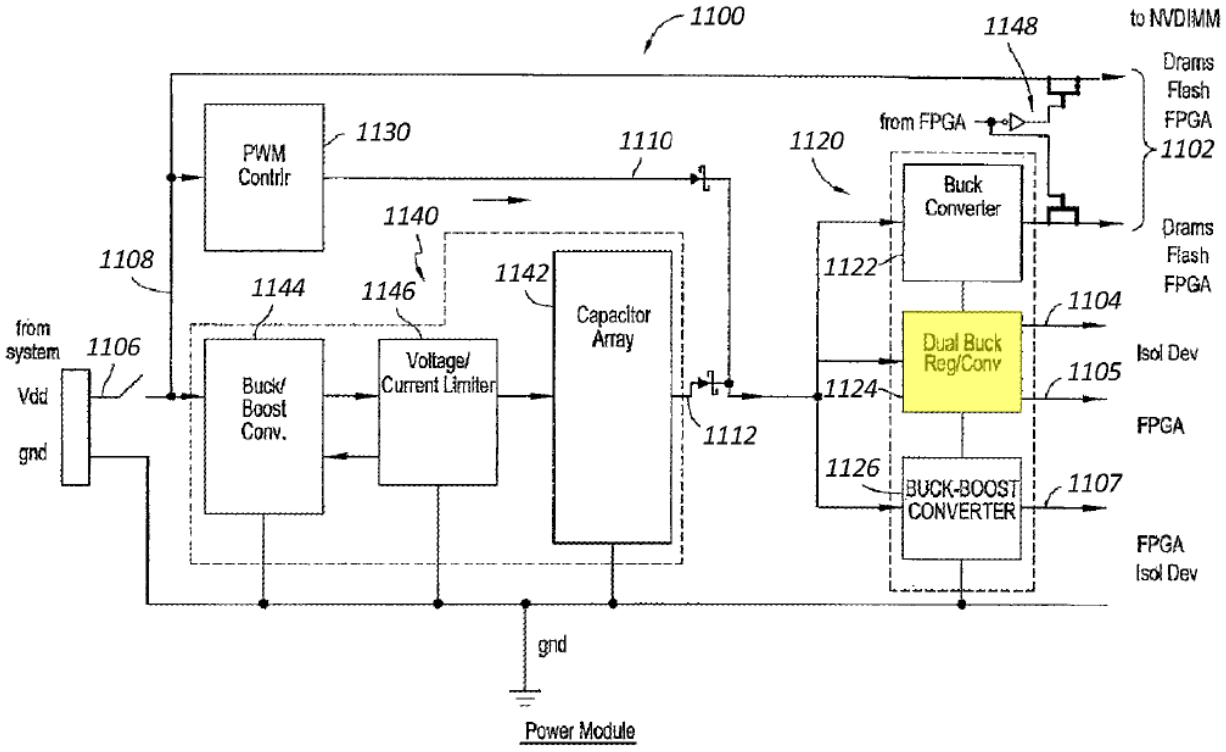
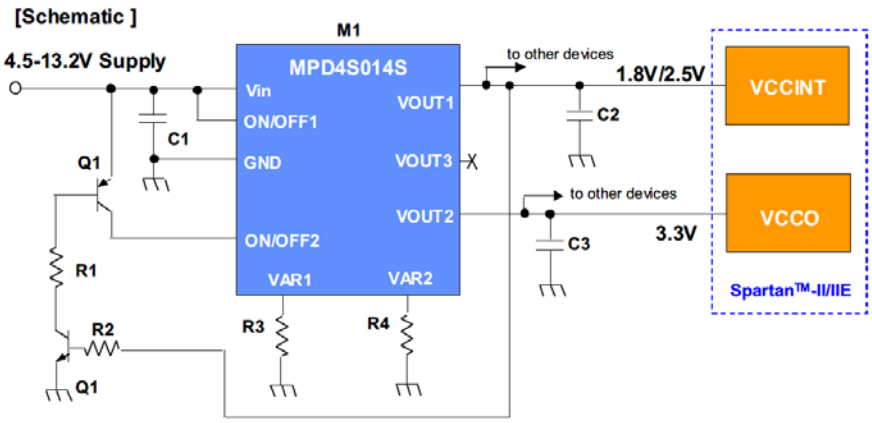


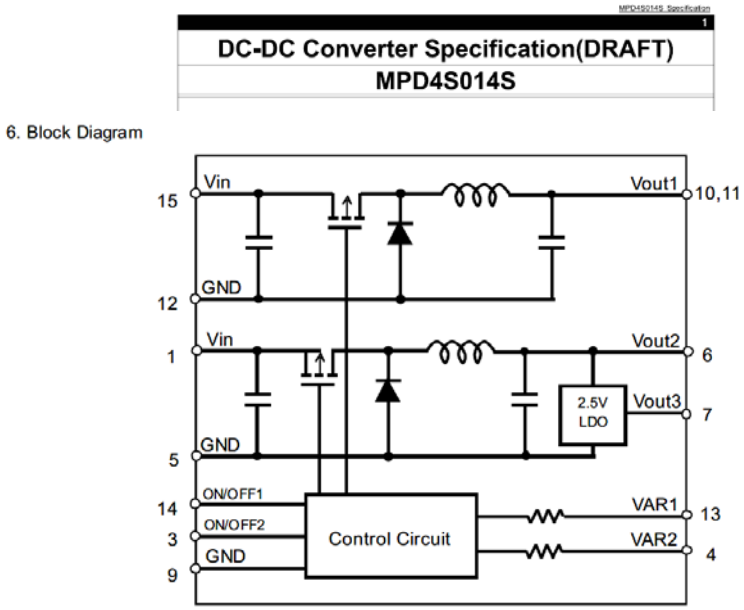
FIG. 16

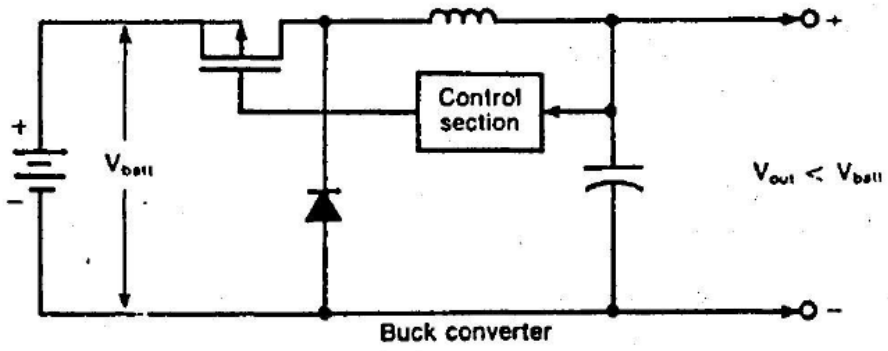
EX1001, 29:28-29, Fig.16 (1124).

At the time, there were many commercially available products that could output ***two*** (or more) regulated voltages using buck converters, and thus in Grounds 1A-1C it would be obvious to implement any two (or more) of the regulated voltages (such as the "*first*" and "*third*") as a "*dual buck converter*" to reduce the number of integrated circuits, pins, and interconnections on the module, therefore simplifying the design. EX1003, ¶338.

For example, Murata offered a MPD4S014S dual buck converter with two different output voltages (e.g., 1.8V and 3.3V, similar to Ground 1B):



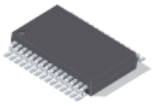




EX1042, p.16; EX1048, pp.1-2; EX1058, p.5.

As another example, Texas Instruments offered a TPS51020 "***Dual***" buck converter, e.g., for V_{DDQ} and V_{TT} voltages for DDR or DDR2 memory devices (similar to Ground 1C where "*first*"=V_{DDQ} and "*third*"= V_{TT}):

TEXAS INSTRUMENTS



TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- **Notebook Computers System Bus and I/O**
- **DDR I or DDR II Termination**

EX1040, pp.1, 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT}").

As another example, Fairchild offered a FAN5026 "***Dual-Output*** PWM Controller" with two different outputs (each anywhere from 0.9V to 5.5V), such as 2.5V and 1.8V similar to Ground 1A or 1B, or V_{DDQ} and V_{TT} like Ground 1C:

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

■ DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

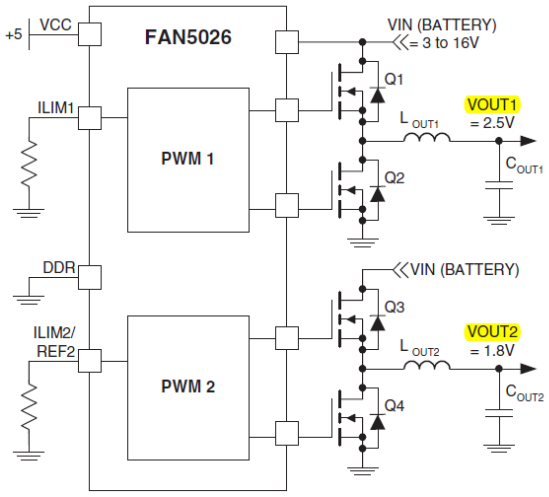


Figure 1. Dual Output Regulator

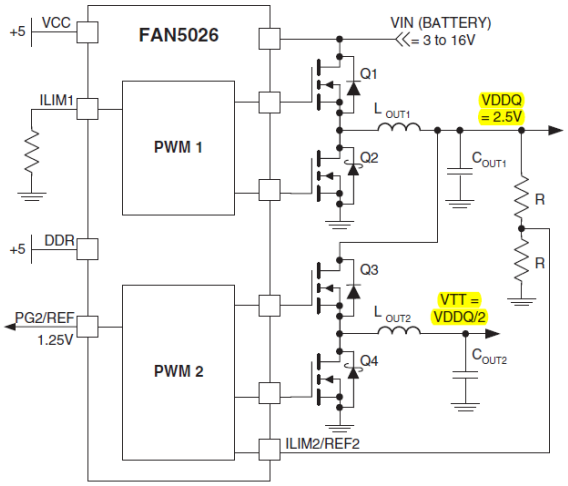


Figure 2. Typical Application

EX1041, pp.1-2, 9; *see also id.*, pp.7-8 (similar).

In short, "*dual buck converters*" were an obvious design choice to simplify the number of parts needed to supply multiple regulated voltages. EX1003, ¶338. An additional motivation to use dual buck converters, like those above, was that the ***phases*** of the two voltages could be adjusted relative to each other, thus

reducing any input "ripple" and improving performance. EX1003, ¶¶342-343; EX1041, p.9; EX1040, p.10; *see also* EX1047, 3:49-50, 4:7-10, 4:37-56, 5:4-13, 5:46-59 & Fig.2 (illustrating dual buck converter with Vout1=V_{DDQ} and Vout2=V_{TT} and phase shifting).

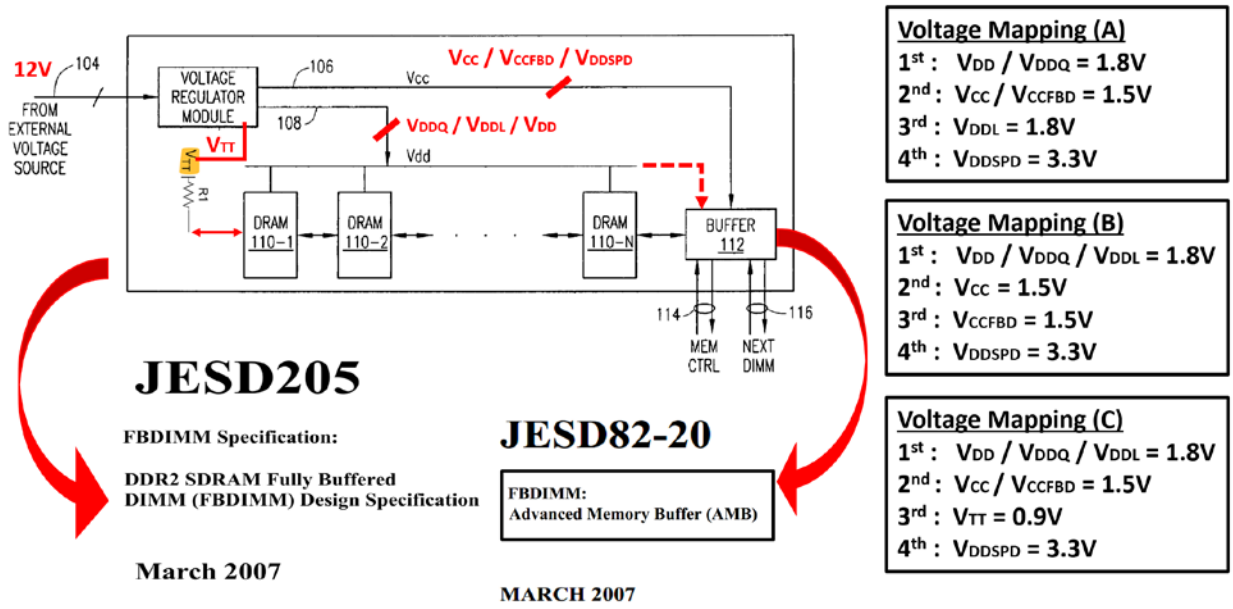
Thus, Grounds 1A-1C teach claim 2.

In litigation, Netlist has pointed to a ***dual-phase*** buck converter (with a ***single*** voltage output, i.e., V_{DD}) as a "*dual buck converter*." EX1071, pp.41, 43; EX1073, pp.49-50. This interpretation is not disclosed in the 918 Patent. EX1003, ¶345. In any event, a ***dual-phase*** buck converter would have been obvious given that Harris specifically teaches using "***multi-phase*** synchronous Pulse-Width Modulated (PWM) controllers." EX1023, ¶[0010]; *see also* EX1032, pp.161-64 (describing use of PWM controllers for buck converters). Such "multiphase buck converter" circuits were known to provide several advantages, including "lower ripple," "higher current capability," and "smaller size." EX1050, 3:36-37, 2:19-20. In light of Harris's express teaching, it would have been obvious to use a ***dual-phase*** buck converter (e.g., for V_{DD}) to reduce ripples and decrease the size of the circuit, thus satisfying Netlist's apparent interpretation for "*dual buck converter*." EX1003, ¶346.

4. Claim 3

Grounds 1A-1C teach "*claim 1, wherein the first voltage amplitude is 1.8 volts*," as shown below and discussed above (pp.14-19, 27). EX1003, ¶¶348-353.

Ground 1: Harris with JEDEC's FBDIMM Standards



5. Claim 8

a) [8.a] Preamble and [8.b] One or More Registers [8.b.1] Coupled to one of the regulated voltages and [8.b.2] configured to register address and control signals

Grounds 1A-1C teach "*claim 1, the plurality of components further comprising: one or more registers* [e.g., in Harris's Buffer, to register incoming signals and output them according to a clock signal, as shown in Figure 3 (below)] *coupled to one of the first, second, third and fourth regulated voltages* [e.g., V_{CC} or V_{CCFBD}, the "*second*" voltage, as discussed above (pp.14-19, 27)], *the one or more registers configured to register, in response to a clock* [e.g., EX1023, ¶[0017] &

Fig.3 (below)], *the first plurality of address and control signals* [from [1.b] and [1.i]]." EX1003, ¶¶393-409.

Harris explains that the "buffer/logic component 112 is provided for ***buffering command/address*** (C/A) space as well as ***data***," EX1023, ¶[0009], which a POSITA would understand involves "*registers*" for registering the address, control, and data signals in response to a "*clock*" signal. EX1003, ¶400; EX1027, p.19 (describing the AMB Buffer as a "DIMM buffer" for "***registering*** outbound ***commands*** and ***data*** at output flops"). As discussed above (pp.22-25), "commands" are sent using "*control*" signals, meaning they both are registered. Harris also discloses that the Buffer uses "*clock*" signals, EX1023, ¶[0017] & Fig.3 (below), which can be used by the "*registers*" in the Buffer. EX1003, ¶¶401-402.

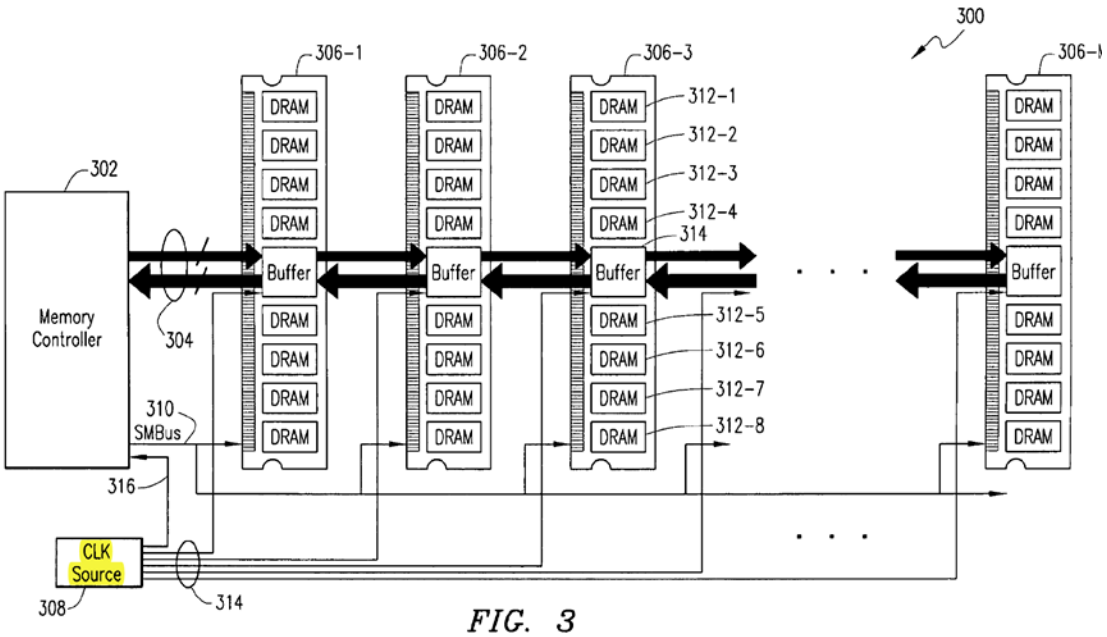
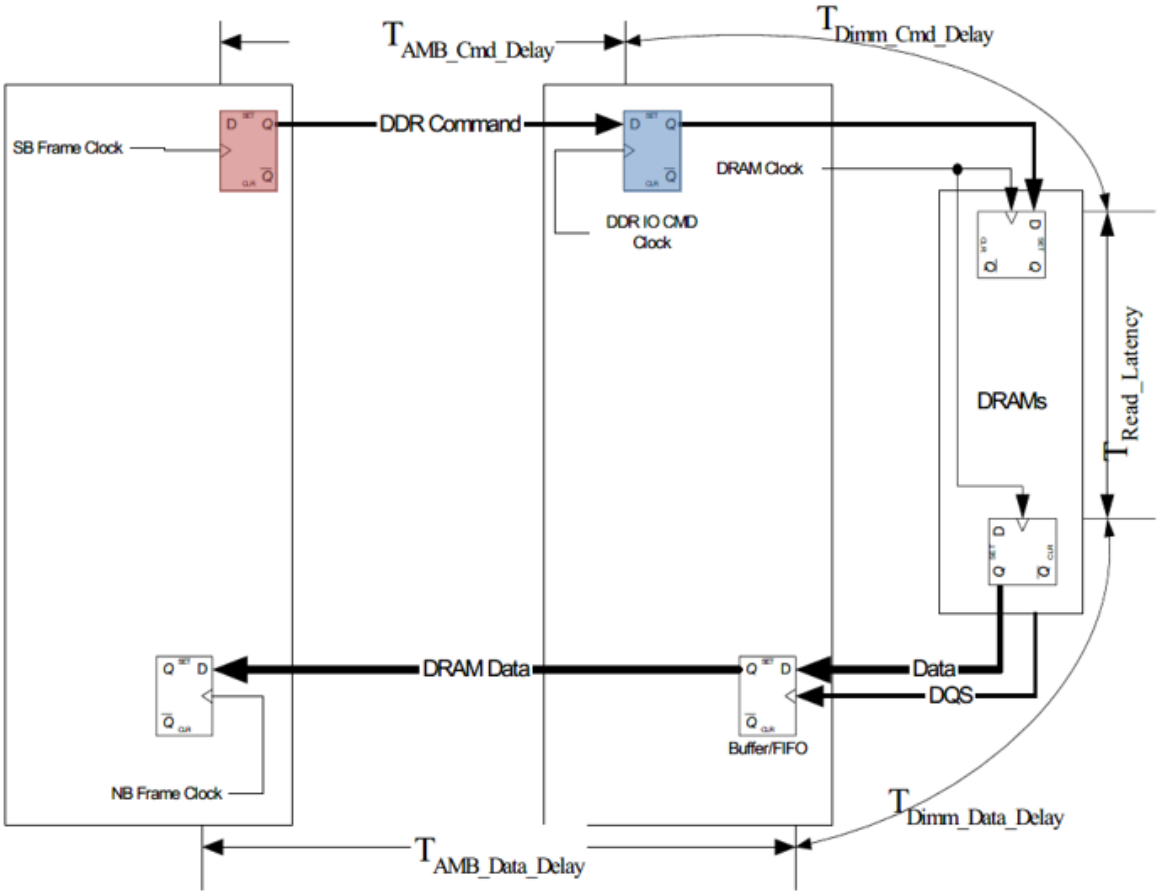


FIG. 3

The use of "*registers*" in Harris's Buffer in response to a "*clock*" is also confirmed by the FBDIMM Standards, which describe an AMB Buffer (like buffer 112 in Harris) that includes "*registers*" (red below), using the "SB Frame Clock" to register DDR address and commands and, (after decoding) forwarding those address and commands to another set of "*registers*" (blue below) which are clocked by a "DDR IO CMD Clock" for interfacing with the DRAM memory devices:

Figure 2.1 — Delays Through an AMB



EX1003, ¶402; EX1027, p.16; *see also id.* pp.3 (showing "Cmd Out" to "DDR IO's" provides "DRAM ***Address/Command***Copy1"), 7 (defining "Resample" and "Resync" to use a "***clock***"), 19 ("FIFO write buffer….fills at half of the DDR data ***rate***, and empties at the DDR data ***rate***"), 20 ("Two sets, or copies, of DRAM ***command and address*** output pins are provided for … ***timing*** considerations."), 59 (showing registers, like the ones above, for "DRAM CMD/ADD"), 82 ("SCK": "AMB ***Clock***").

As discussed above (pp.14-19, 27), Harris discloses that V_{CC} (e.g., the "*second*" voltage) is coupled to the Buffer (and thus the "*registers*"), *e.g.*, EX1023, ¶[0012] & Fig.1A, and the FBDIMM Standards confirm that both V_{CC} and V_{CCFBD} (e.g., another possible "*second*" voltage) are coupled to the input/output (I/O) for the buffer (and thus the "*registers*"), as shown below. EX1003, ¶¶403-405.

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

EX1027, p.83.

Power/Ground Signals		213
V_{CC}	AMB Core Power (1.5 Volt)	24
V_{CCFBD}	AMB Channel I/O Power (1.5 Volt)	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt)	24
V_{DDSPD}	SPD Power (3.3 Volt)	1
V_{SS}	Ground	156

EX1028, p.30.

b) [8.b.3] Wherein one of the voltages is selectively switched off

Grounds 1A-1C teach "*wherein the one of the first, second, third and fourth regulated voltages* [e.g., 1.5V for V_{CC}/V_{CCFBD}, the "*second*" voltage, which powers the input/output "*registers*" of Harris's Buffer, as discussed immediately above] *is selectively switched off to turn power off to the one or more registers* [e.g., in S3 sleep mode for FBDIMMs] *while one or more components of the plurality of components* [e.g., the DRAMs] *are powered on* [e.g., with V_{DD}=1.8V (pp.14-19, 27) to refresh the data in the DRAMs during S3 sleep mode]." EX1003, ¶¶410-411, 414-420.

Harris can be implemented on an FBDIMM, EX1012, ¶[0009], which a POSITA would know has an "S3 sleep mode" to save power "in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode." EX1027, p.39; EX1003, ¶¶414-415, 419. In particular, "in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low [i.e., they are not used, so there is no need to "*register*" them]…. 1.8V supply is on [i.e., for V_{DD} to the DRAMs, *see* pp.14-19, 27]. 1.5V [i.e., for V_{CC}/V_{CCFBD} to the I/O of the Buffer, *see* pp.14-19, 27], Vtt, and 3.3V are off. DRAMs are in self refresh [i.e., still powered on with V_{DD}=1.8V], and the CKE signals must be driven low." EX1027, p.21. Thus, a

POSITA would have known (and been motivated, with a reasonable expectation of success) to selectively switch off power to the interface of the Buffer (including the "*registers*" and corresponding analog circuitry), because that would provide an enormous "power saving" opportunity. EX1033, 1:51-53, 9:57-60, 12:50-58; *see also* EX1039, ¶[0065] (describing turning off AMB Buffer to conserve power). A POSITA would also have known that power to the "*registers*" could be turned off either by turning off the relevant buck converter (to save maximum power) or with a switch to selectively allow/prevent V_{CC}/V_{CCFBD} from reaching the "*registers*" (to avoid any delays with restarting the buck converter when power is turned back on). EX1003, ¶413; EX1056, Abstract, 3:5-11, 5:15-26 ("switch"), Fig.3.

6. Claim 14

Grounds 1A-1C teach "*claim 8, wherein, in response to selectively switching on* [e.g., when S3 sleep mode discussed in [8.b.3] ends and "normal DRAM transactions begin" again, EX1027, p.25] *the one of the first, second, third and fourth regulated voltages to the one or more registers* [e.g., 1.5V for V_{CC}/V_{CCFBD}, the "*second*" voltage, which powers the input/output "*registers*" of Harris's Buffer, as discussed in [8.b.1]], *the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices* [e.g., as discussed in [1.i.2] and [8.b.2] for normal operation]." EX1003, ¶¶462-466.

7. Claim 15

Grounds 1A-1C teach "*claim 1, the plurality of components further comprising: a logic element* [e.g., logic in Harris's Buffer] *including one or more integrated circuits* [e.g., an integrated circuit within Harris's Buffer, and an integrated circuit, like an SPD, including non-volatile memory] *and discrete electrical elements* [e.g., resistors and/or capacitors to terminate voltages for Harris's Buffer], *the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information* [e.g., S3 Recovery Configuration Registers as required by S3 sleep mode, EX1027, p.25]." EX1003, ¶¶468-476; *see also id.* ¶¶435-437.

An FBDIMM, like Harris's memory module, will "*store configuration information*" in "*non-volatile memory*" before entering into S3 sleep mode. EX1027, pp.25 ("The following CSRs [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin…."), 95-96, 141 ("S3RESTORE" registers).

Harris teaches that his Buffer has "*logic*" and thus is referred to as "buffer/***logic*** component 112." EX1023, ¶[0009]. A POSITA would have understood this "*logic element*" to include "*one or more integrated circuits*," such as an integrated circuit within the buffer 112, and an integrated circuit like an SPD

("Serial Presence Detect," EX1028, p.105). *Id.*; EX1003, ¶474. For example, Harris illustrates the Buffer as a chip with integrated circuits in Figure 3:

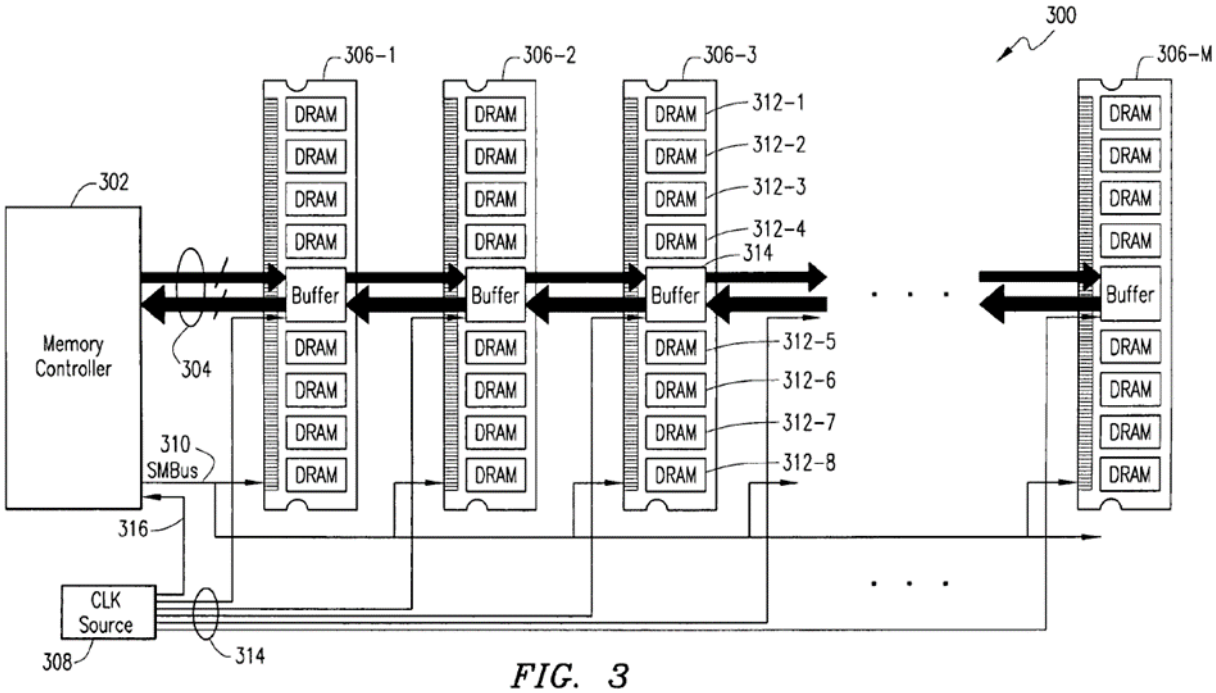
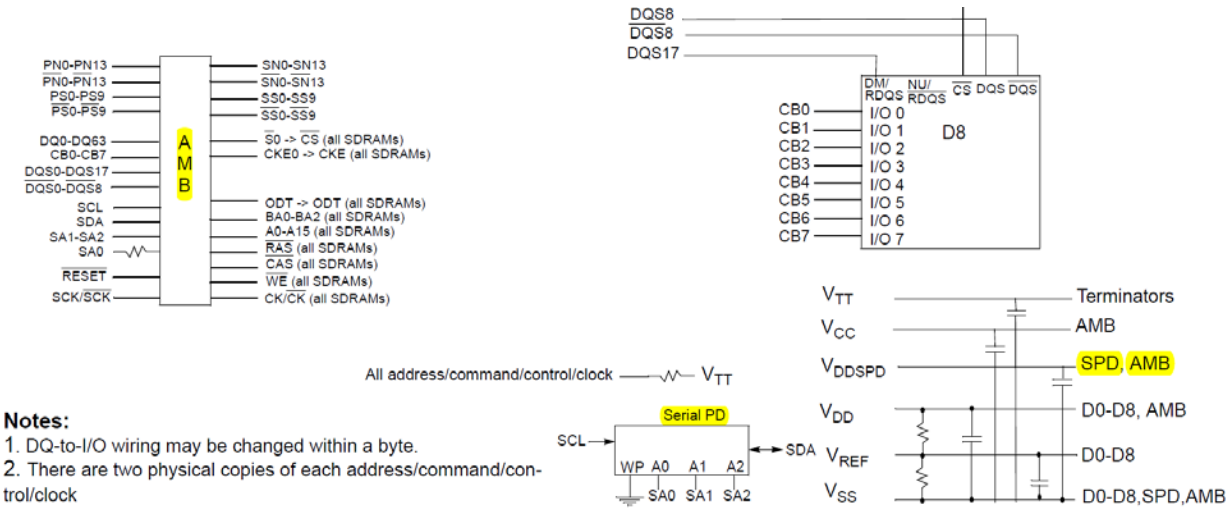


FIG. 3

EX1023, Fig.3. Furthermore, a POSITA would have understood that the "*non-volatile memory*" can be implemented in the SPD device, separate from the integrated circuit implementing the "AMB" Buffer, as shown below, where the SPD is used to "*store configuration information*" in "*the non-volatile memory*":



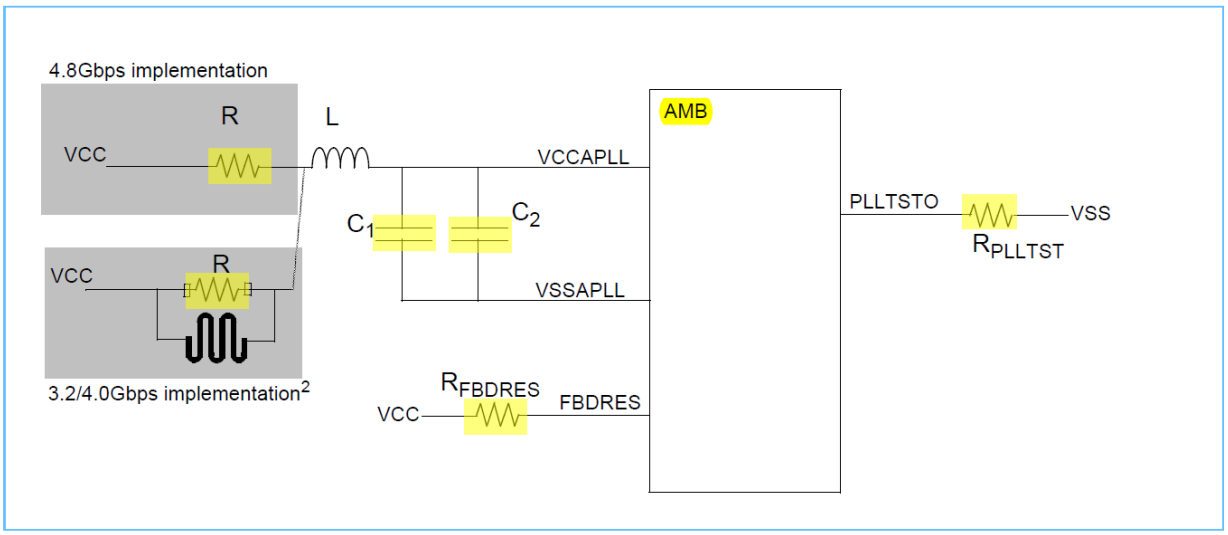
Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

EX1028, p.13; *see also* EX1027, p.117 ("SPD EEPROM" for storing settings); EX1066, 26:64-27:4 (describing storing configuration information in an SPD). In the alternative, given that V_{DDSPD} is also supplied to the AMB Buffer (as shown above right), it also would be obvious to a POSITA that the claimed "*non-volatile memory*" could be contained in the Buffer, thus decreasing the number of components, interfaces, and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. EX1003, ¶436; EX1066, 26:64-27:4 (describing in the alternative storing configuration information "on the buffer or controller device"); EX1067, p.1-1 (FPGA logic with internal non-volatile memory); EX1023, ¶¶[0019] (discussing benefits of reduced pin count).

A POSITA would have also understood that the "*logic element*" in Grounds 1A-1C includes "*discrete electrical elements*," such as resistors and capacitors. EX1003, ¶475. For example, Harris discloses interfaces on the Buffer, such as bidirectional memory controller interfaces (114, 116), EX1023, ¶[0009] & Fig.1A,

which would include resistors and capacitors according to the FBDIMM Standards:

PLL and Channel Bias



NOTE 1: There is no connection to ground from VSSAPLL.
NOTE 2: Users must ensure AMB requirements are met by their implementation. Example, in VCCAPLL network, R implemented as copper trace serpentine may not achieve acceptable tolerances for all AMBs.
NOTE 3: VCC power delivery requirements (as specified for VCC balls) are assumed to be met at inputs of VCCAPLL and FBDRES networks, not at VCCAPLL and FBDRES balls.

EX1028, p.43; *id.*, pp.42-45. Furthermore, the voltages to and from the "*logic element*" must be terminated, conditioned, and set as required to operate properly, EX1003, ¶475, and the FBDIMM Standards disclose that the voltages to the AMB Buffer and/or SPD (e.g., V_{TT}, V_{CC}, V_{DDSPD}, V_{DD}) are terminated, conditioned, and set using resistors and/or capacitors, EX1028, p.13 (bottom right figure).

8. Independent Claim 23

The limitations of claim 23 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Grounds 1A-1C for at least the same reasons discussed above:

This limitation in claim 23…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[23.a]	[1.a]	¶¶558-561 (¶¶216-222)
[23.b]	[1.b]	¶¶562-565 (¶¶223-231)
[23.c.1]	[1.g]	¶¶566-569 (¶¶288-297)
[23.c.2]	[1.h], [1.i.1], [1.i.3], [8.b.1]	¶¶570-573 (¶¶298-310, 318-323, 398-405)
[23.c.3]	[1.i.2], [8.b.2]	¶¶574-577 (¶¶311-317, 406-409)
[23.d]	[1.c], [1.d], [1.e]	¶¶578-581 (¶¶232-280)
[23.e]	[1.f]	¶¶582-585 (¶¶281-287)
[23.f]	[8.b.3], [14]	¶¶586-589 (¶¶410-420, 462-466)
[23.g]	[14]	¶¶590-593 (¶¶462-466)
[23.h]	[8.b.3][3]	¶¶594-597 (¶¶410-420)

B. Ground 2

Ground 2 renders obvious claims 1-30.

[3] A POSITA would have understood that, in S3 sleep mode, when the registers are not powered and address and control lines are driven low as discussed in [8.b.3], *see* EX1027, p.21, the result is that "*the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals*" as required by [23.h]. EX1003, ¶597.

1. Ground 2 combination: Ground 1 + Amidi (EX1024)

Ground 2 combines Ground 1 (Harris with the FBDIMM Standards) with Amidi (shown in blue below) as follows:

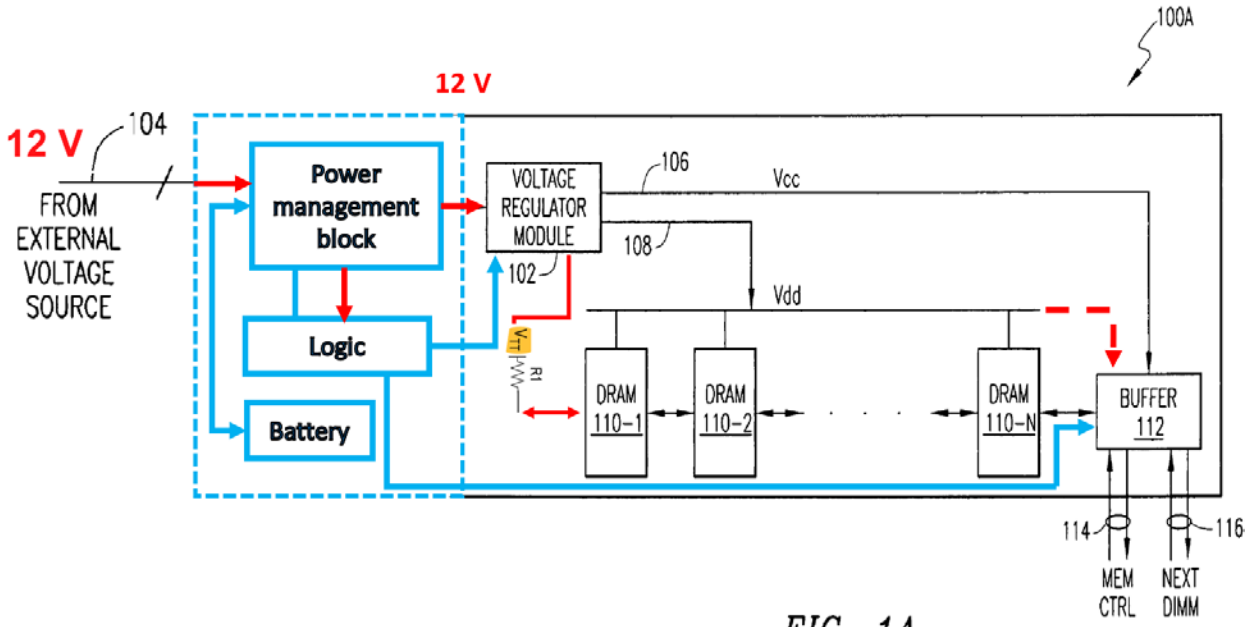


FIG. 1A

EX1003, ¶¶170-179. As explained below, Amidi teaches battery backup to provide power to Harris's memory module during a power disruption. The "Logic" of Amidi (blue above) can detect power disruptions, switch to battery power, and preserve data in the DRAMs by sending "self-refresh" commands.

A POSITA would have been motivated to combine Ground 1 with Amidi, and had a reasonable expectation of success in doing so, because Harris recognizes concerns with power reliability and proposes adding a "redundant" power source, EX1023, ¶¶[0014, 16], Figs.1B, 2, while Amidi teaches such a redundant power source (e.g., a battery on the memory module) for maintaining data during a power

disruption, EX1024, Abstract, 1:28-35, 2:6-26, 4:14-60, Figs.5-6, 14-15; EX1003, ¶¶170-175. The "power management block" of Amidi (above left, in blue) could be modified easily to work with the FBDIMM memory module of Harris, as shown in the annotated version of Figure 5 of Amidi below:

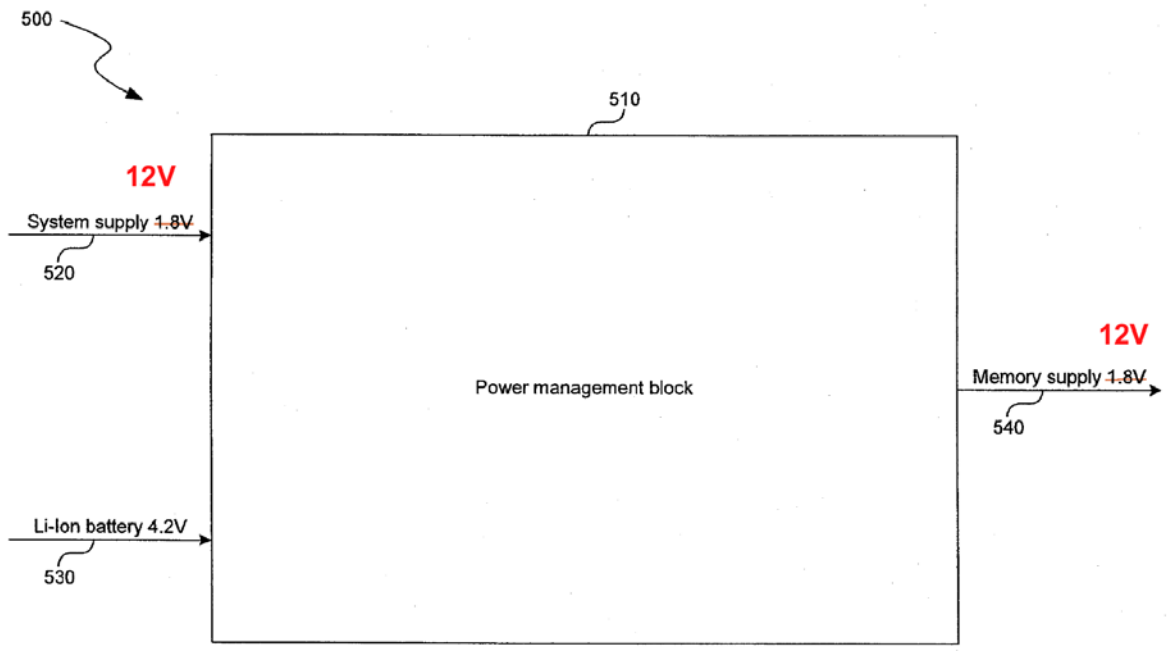


FIG. 5

EX1024, Fig.5 (annotated with teachings of Harris); EX1003, ¶¶171-172. Harris teaches using a 12V external supply, EX1023, ¶[0012], so in the Ground 2 combination, it would have been obvious to a POSITA that the 12-volt external supply (above left) is stepped-down with a buck converter to a 5-volt supply for Amidi's lithium-ion battery charger (EX1024, Fig.6 (620), not shown above), and Amidi's battery voltage (e.g., 4.2 volts, above left) is stepped-up with a boost converter to the 12-volt level used by Harris's memory module (above right).

EX1003, ¶¶171-172. Indeed, Amidi expressly discloses that his "power management block" (Fig.5 above) uses "buck" converters to step-down voltages as needed, *see, e.g.*, EX1024, 4:38-40 & Fig.6 (640 "buck"), and "boost" converters to step-up voltages as needed, *id.*, 4:27-32 & Fig.6 (610 "boost"), as had long been taught in textbooks, *see, e.g.*, EX1058, p.3 ("buck," "boost"); EX1032, p.161 (same).

Furthermore, Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module discussed above (pp.45-46), providing another motivation to combine Ground 1 with Amidi. Both modes put the SDRAMs in a self-refresh state to preserve data while conserving power. *Compare* pp.45-46, *with* EX1024, Fig.11, 2:16-19 ("Similarly, one may provide a process which operates to … maintain memory (through refresh, for example)"). Thus, a POSITA would have been motivated to use the teachings of S3 mode in Ground 1 when implementing Amidi's backup power supply and logic functionality. EX1003, ¶173. Indeed, the S3 mode was described in the FBDIMM Standards for the very purpose of saving power in all types of computers, including servers and workstations. EX1027, p.39 ("very lower power state"); EX1028, p.9 ("FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations.").

Thus, a POSITA would have been motivated to implement Harris's FBDIMM memory module with the functionality of Amidi's power management and logic blocks for detecting power disruptions and switching over to battery backup when needed. EX1003, ¶¶170-174. This straightforward modification of Harris's memory module in view of Amidi and the knowledge of a POSITA simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to provide a backup power supply using a battery). *Id.*, ¶175. In addition, the modification merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for improvement to yield predictable results (e.g., redundancy when the system supply or clock fails). *Id.*

As summarized in the annotated figures below showing the combination for Ground 2, Amidi's "power management block" (blue, below left) supplies the voltages for Amidi's logic and for Harris's Voltage Regulator Module, which in turns supplies the voltages for various components on the FBDIMM memory module as specified by the FBDIMM Standards, including those listed below on the right. EX1003, ¶¶174-179.

Ground 2: Ground 1 and Battery Backup of Amidi

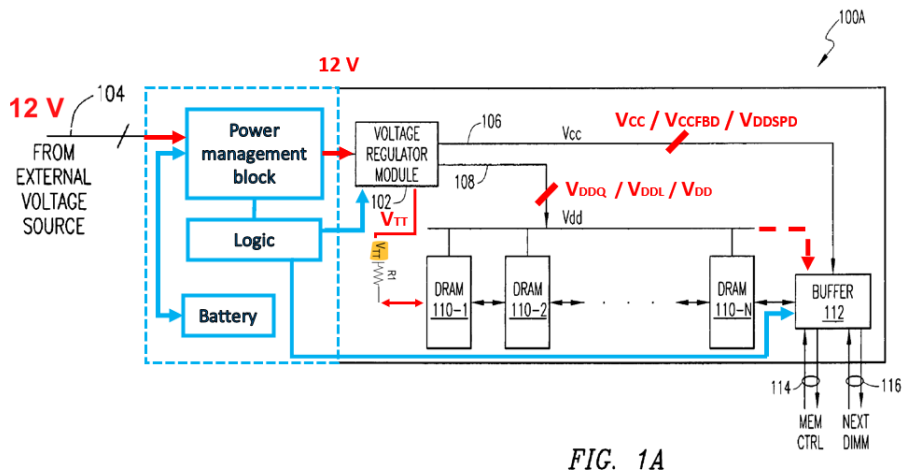


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Voltage Mappings "A" to "C" (on the right, referred to as Grounds 2A-2C) are simply different ways to apply the arbitrary labels "1st" through "4th" to the voltages shown in red in the annotated figures. EX1003, ¶¶174-179. Grounds 2A-2C involve the same voltage mappings as Grounds 1A-1C above (pp.14-19, 27). *Id.*

2. Claims 1-3, 15, 23

For claims 1-3, 15, and 23, Grounds 2A-2C have the same voltage mappings as Grounds 1A-1C, and the addition of Amidi in Grounds 2A-2C does not negate any of the arguments in Grounds 1A-1C for those claims, and thus Grounds 2A-2C invalidate those claims for at least the same reasons provided above for Grounds 1A-1C. EX1003, ¶¶215-353, 467-476, 557-597.

3. Claim 4

Claim 4 requires "*claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively*." EX1003, ¶¶354-358. As explained above (p.27), Harris discloses the range of 0.5V to 3.3V, thus rendering the specific voltages of claim 4 within that range obvious under Federal Circuit precedent.

Claim 4 is also obvious in light of the following voltage mapping, referred to as "Ground 2D":

Ground 2: Ground 1 and Battery Backup of Amidi

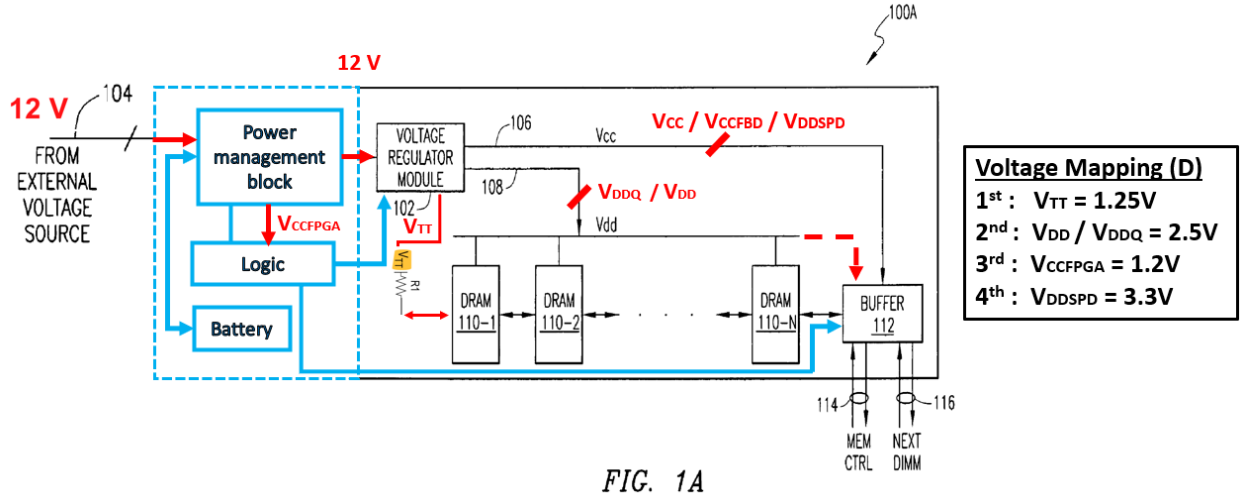


FIG. 1A

Ground 2D involves the following voltage mappings assuming "DDR" DRAM at 2.5V as taught by Harris, EX1023, ¶¶[0002, 9] & Fig.1A, and consistent with the JEDEC standard for "DDR" memory, EX1045, pp.1 ("VDD = … 2.5 V"), 7, 54.

- 1.25V for **V_{TT}** to the resistors, "DDR" DRAM (110-1 to 110-N above), and "AMB" Buffer (112 above).
- 2.5V for **V_{DD}/V_{DDQ}** to the DRAM and Buffer.
- 1.2V for **V_{CCFPGA}** to Amidi's logic (blue, above left), which could be a Xilinx FPGA with a 1.2V supply, *see, e.g.*, EX1024, 2:12-16, 6:40-43; EX1025, ¶[0037]; EX1042, p.2 (1.2V for Xilinx FPGA); EX1044, Fig.8 (1.2V for FPGA); EX1043, p.1 (1.2V for FPGA); EX1003, ¶¶278-279.
- 3.3V for **V_{DDSPD}** to the Buffer and the SPD (not shown above).

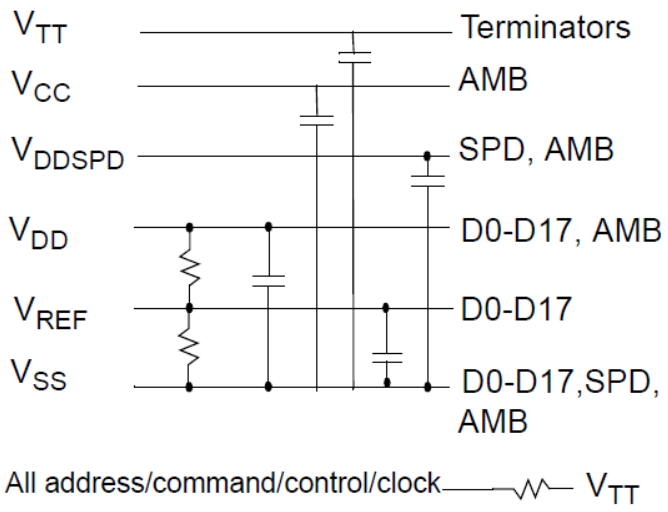
See EX1003, ¶179; EX1023, ¶¶[0002, 9-10], FIG.1A; EX1045, pp.1, 7, 54 (below), 60 (V_{DD}, V_{DDQ}, V_{TT}); EX1028, p.9 (V_{TT}=0.5*V_{DD}).

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7

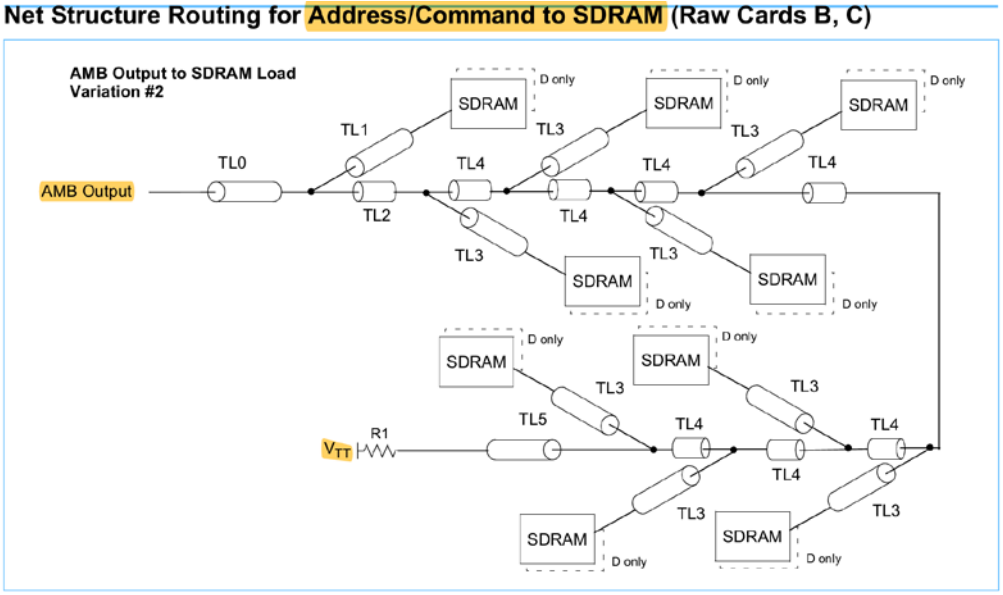
See also EX1042, p.2 (V_{CCFPGA}, labeled V_{CCINT} below).

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

See also EX1027, pp.32, 83 (V_{DDSPD}=3.3V); EX1023, ¶[0017], FIG.3; EX1028, p.15:



Id., p.68:



Ground 2D also teaches claims 1-2 and 15 for substantially the same reasons provided above for Grounds 1A-1C, except with the following voltage mapping:

	Voltage Mapping D (Grounds 2-3)
"*first*":	V_{TT}=1.25V
"*second*":	V_{DD}/V_{DDQ}=2.5V
"*third*":	V_{CCFPGA}=1.2V
"*fourth*":	V_{DDSPD}=3.3V

See supra pp.57-59. This voltage mapping satisfies all the limitations of claims 1-2 and 15, including the specific voltage-related limitations below:

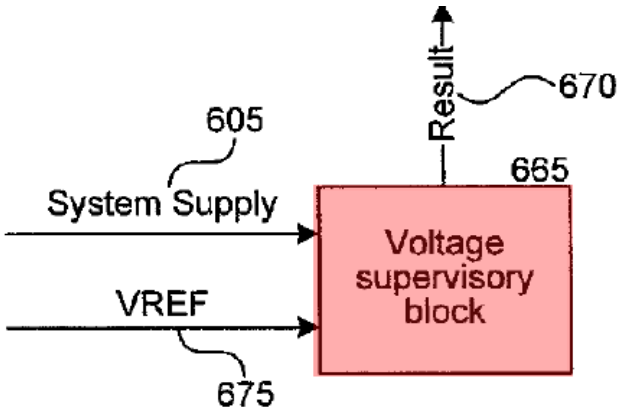
- [1.h] (SDRAM "*coupled to the first regulated voltage*"). *See supra* pp.57-59.
- [1.i.3] (Buffer coupled to both "*second*" and "*fourth*" voltages). *Id.*
- [1.i.4] ("*second*" and "*fourth*" amplitudes are different). *Id.*
- [2] ("*first*" and "*third*" configured to operate as a "*dual buck converter*"). *See supra* pp.35-40 (explaining obviousness of "*dual buck converter*").

4. Claim 5

Grounds 2A-2D teach "*claim 1, further comprising a voltage monitor circuit* [e.g., Amidi's voltage supervisory block 665] *configured to monitor a power input voltage* [e.g., system supply 605] *received via a second portion of the plurality of edge connections* [see [1.b]]" and "*produce a trigger signal* [e.g., to switch to battery power] *in response to the power input voltage having an amplitude that is*

greater than a first threshold voltage [e.g., overvoltage protection]." EX1003, ¶¶359-376.

Amidi's "voltage supervisory block" 665 (red, below) is a "*voltage monitor circuit*" that can detect power disruptions, including undervoltage conditions such as a power failure, and "*produce a trigger signal*" (670) to switch to battery power, as shown in Figure 14. EX1024, 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6 (excerpted below), 14 (below), 15.



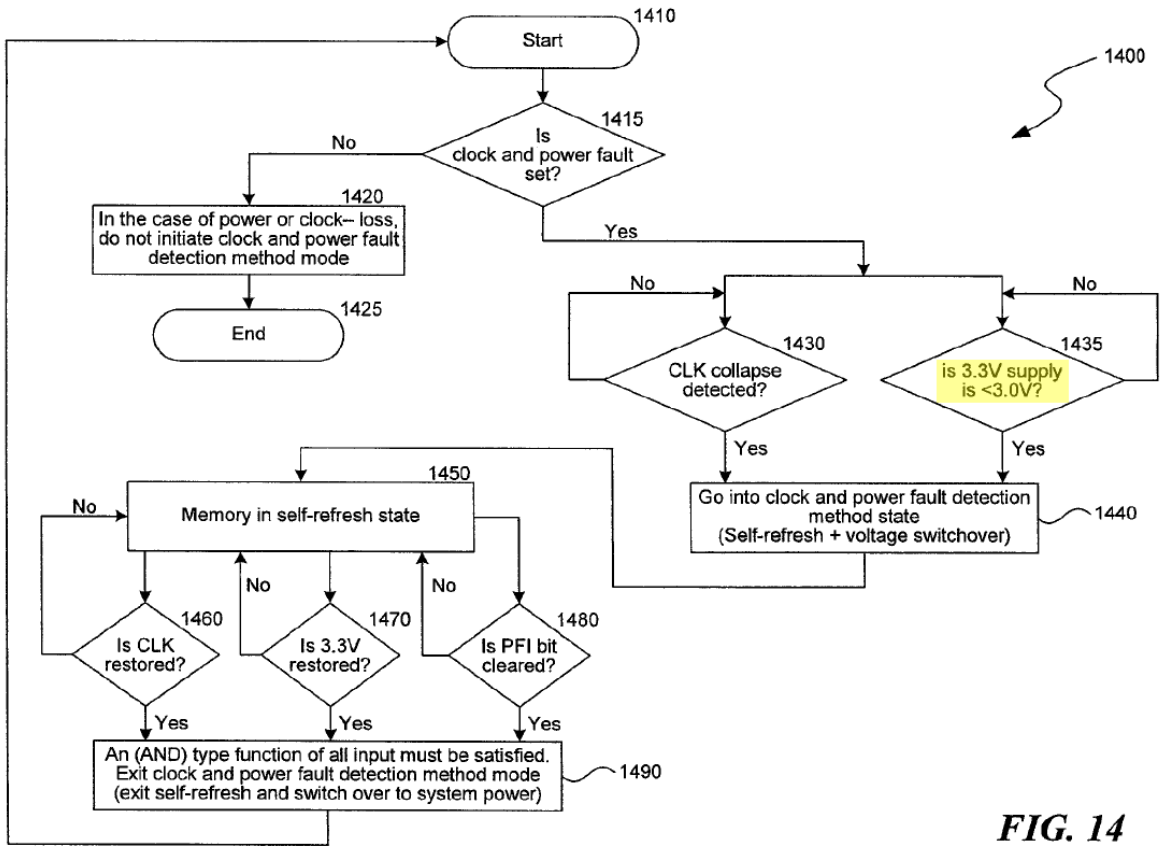


FIG. 14

Additionally, Harris teaches ***both*** overvoltage ***and*** undervoltage protection of "+/- 15%." EX1023, ¶[0013]. Thus, in the combination of Ground 2, a POSITA would have been motivated by Harris to include overvoltage protection ("*amplitude that is greater than a first threshold voltage*") in Amidi's "*voltage monitor circuit*" shown above, with a reasonable expectation of success. EX1003, ¶¶368-374. Indeed, such circuitry for ***both*** overvoltage ***and*** undervoltage protection was well known and commercially available:

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 μF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar).

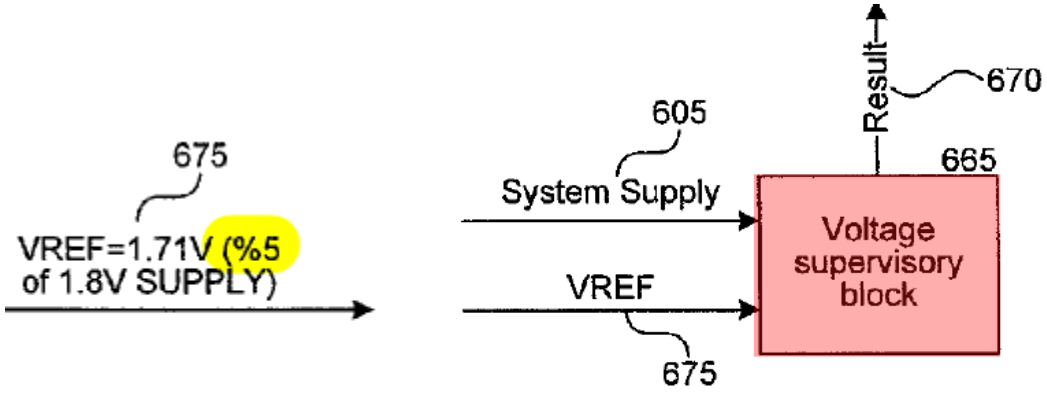
5. Claim 6

As explained directly above for claim 5, Grounds 2A-2D also teach undervoltage protection, as required by claim 6: "*claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage*." EX1003, ¶¶377-384.

6. Claim 7

Grounds 2A-2D teach "*claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating*

voltage [e.g., 12 volts for Harris's external supply 104]." EX1003, ¶¶385-392. The claimed threshold of "*ten percent*" is within the range of thresholds disclosed in the prior art, and thus obvious under Federal Circuit precedent discussed above (p.27). In particular, Harris teaches a threshold of "+/-15%," EX1023, ¶[0013], so under Federal Circuit precedent, any threshold in the range of 15% under to 15% over would have been obvious. Furthermore, Amidi teaches an undervoltage threshold of 5% (below), making the range of 5% under to 15% under even more obvious. EX1003, ¶390.



…

EX1024, 4:44-55, Fig.6 (675). A POSITA would have understood that a tolerance around 10% provided a reasonable compromise between the risk of losing data, or damaging devices, from too high a tolerance, and of unnecessary interruptions from too low a tolerance. EX1003, ¶390. Indeed, thresholds around 10% for undervoltage and/or overvoltage were known, as shown by Amidi, the FBDIMM Standards, and commercially available products:

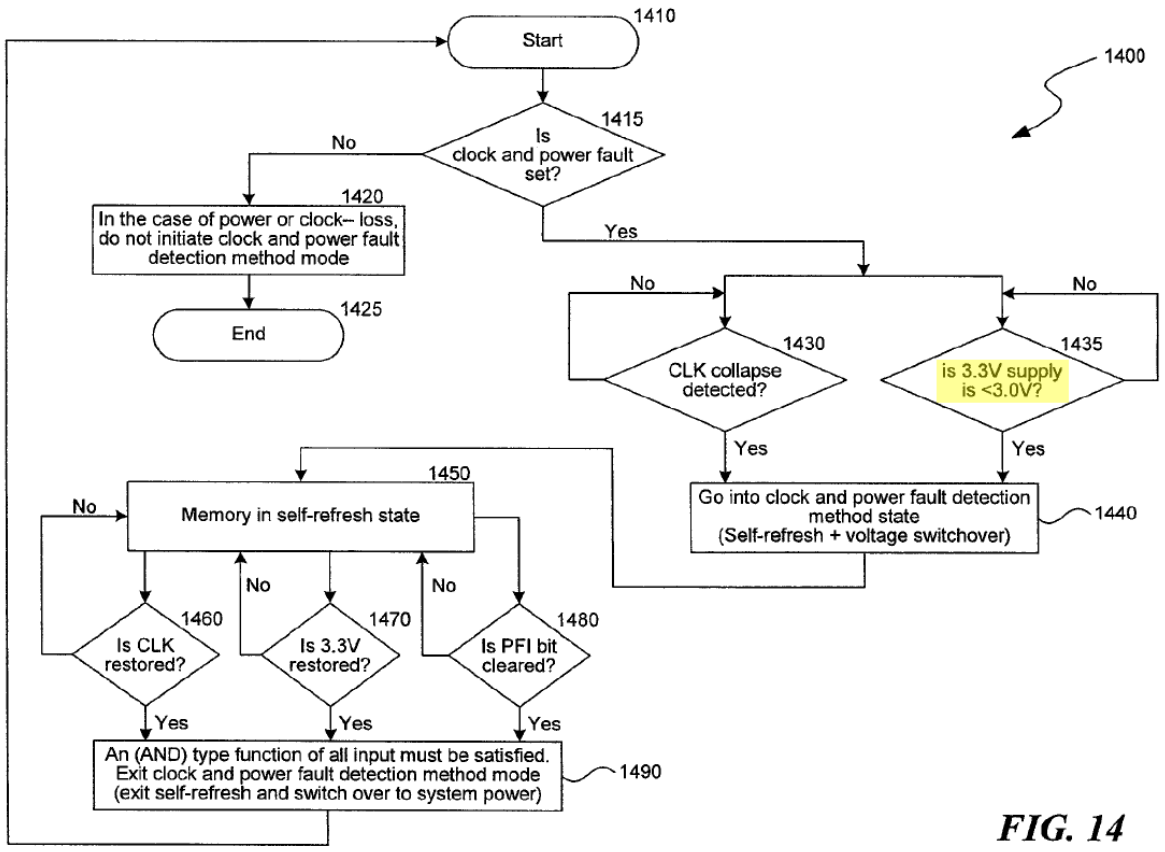


FIG. 14

EX1024, 8:23-36, Fig.14.

Table 4.2 — Advanced Memory Buffer Normal Mode DC Electrical Parameters

Parameter		Units	Min	Typ	Max
V_{CC} link / core	0kHz - 30kHz	Volts	1.455	1.5	1.575
V_{DD}		Volts	1.7	1.8	1.9
V_{DDSPD}		Volts	3.0	3.3	3.6

EX1027, p.32.

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PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 μF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1061, p.15 (programmable under- and over-voltage protection over a range, including 10%).

7. Claims 8, 14

Grounds 2A-2C render obvious claims 8 and 14 for at least the same reasons provided for Grounds 1A-1C above (pp.41-46). In addition, Amidi in the combination for Grounds 2A-2C further renders obvious [8.b.3] by teaching that, in a power failure, the system address and control signals are disconnected from the memory module, and the SDRAM are controlled by a state machine that generates refresh commands, EX1024, 7:24-34, Fig.12 (below), providing an additional motivation to "*turn power off to the one or more registers*" since there would not be any address or control signals to "*register*" during the power failure, and doing so would extend the battery backup power. EX1003, ¶¶412-413.

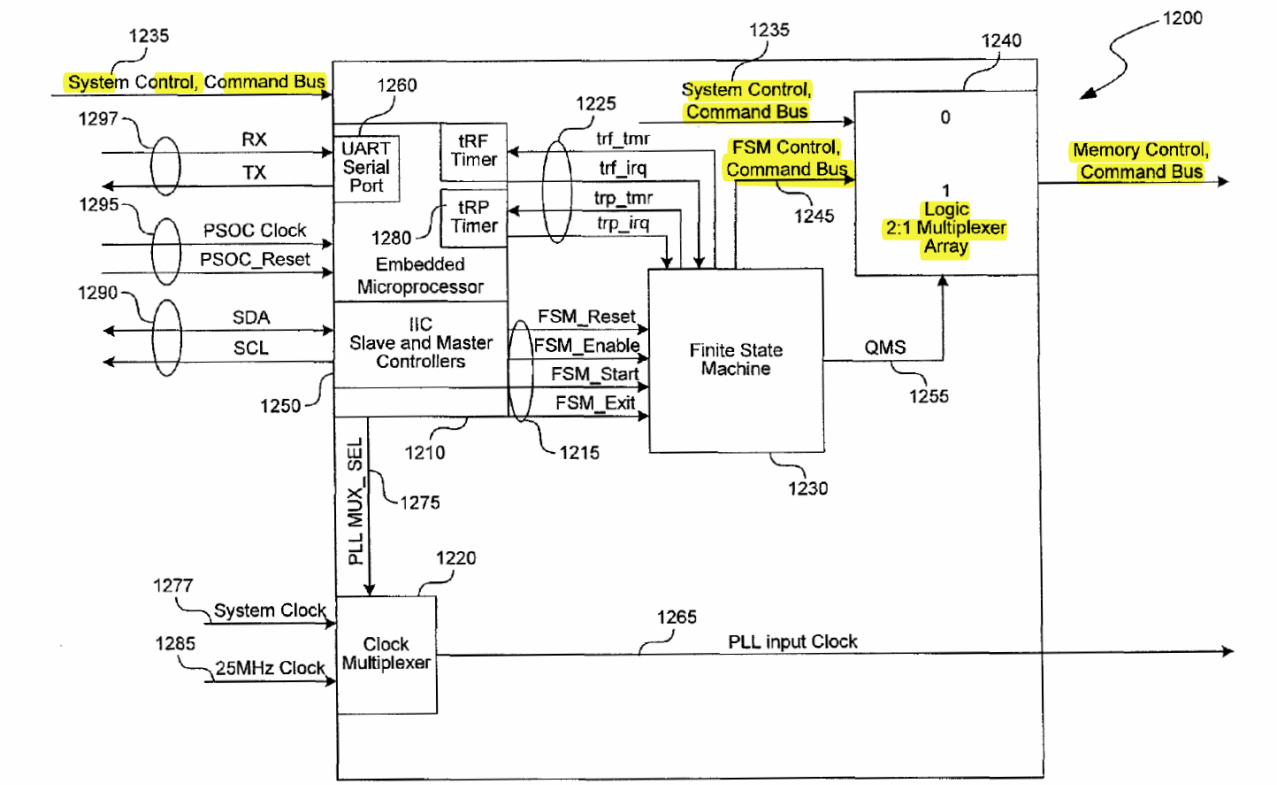


FIG. 12

8. Claim 9

As explained for claims 5 to 7 above (pp.60-66), Grounds 2A-2D also teach overvoltage protection with a 10% threshold, as required by claim 9: "*claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*." EX1003, ¶¶421-426.

9. Claim 10

Grounds 2A-2D teach "*claim 5, the plurality of components further comprising: a logic element* [e.g., logic in Harris's Buffer] *including a non-volatile memory, the non-volatile memory is configured to store configuration information* [e.g., S3 Recovery Configuration Registers as required by S3 sleep mode, EX1027,

p.25]." EX1003, ¶¶427-438. These limitations of claim 10 are also found in claim 15, and thus Grounds 2A-2D teach claim 10 for substantially the same reasons that Grounds 1A-1C teach claim 15 as discussed above (pp.47-50).

10. Claim 11

Grounds 2A-2D teach "*claim 10, wherein, in response to the trigger signal* [see claim 5, e.g., from a power disruption], *the logic element writes information into the non-volatile memory* [e.g., S3 configuration information as discussed above in claims 10 and 15, to allow sleep mode, thus conserving power during Amidi's battery backup mode]." EX1003, ¶¶439-443. As discussed above (p.54), Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module, because both modes put the SDRAMs in a self-refresh state to preserve data while conserving power. *Compare* pp.45-46, *with* EX1024, Fig.11, 2:16-19 ("Similarly, one may provide a process which operates to … maintain memory (through refresh, for example)"). Thus, in the event of a power disruption causing a "*trigger signal*," a POSITA would have been motivated to use the S3 sleep mode discussed above in claim [8.b.3] (pp.45-46) to conserve power during Amidi's battery backup mode, and as discussed in claims 10 (p.67) and 15 (pp.47-50), S3 sleep mode requires writing S3 configuration information "*into the non-volatile memory*" before going to sleep. EX1003, ¶442.

11. Claim 12

a) [12.a] Preamble and [12.b] A Non-Volatile Memory

As discussed above for claims 10-11 (pp.67-68) and claim 15 (pp.47-50), Grounds 2A-2D teach "*claim 5, the plurality of components further comprising: a non-volatile memory; and….*" EX1003, ¶¶444-452.

b) [12.c] A Controller performs a write operation

Grounds 2A-2D further teach, at least under Netlist's apparent interpretation of the claim, EX1071, pp.39-46; EX1073, pp.46-63, "*a controller* [e.g., in Harris's buffer] *configured to receive the trigger signal* [see claim 5, e.g., from a power disruption], *wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory* [e.g., S3 configuration information is stored in non-volatile memory before entering S3 sleep mode, as discussed for claim 11 (pp.68-68)]." EX1003, ¶¶453-456.

12. Claim 13

Grounds 2A-2D teach "*claim 5, wherein the power input voltage* [e.g., 12V] *is coupled to the first, second, and third buck converters and the converter circuit* [e.g., in Harris's voltage regulator module 102, as shown below and discussed above for [1.c]-[1.f] in Grounds 1 and 2 (pp.26-31, 52-60) when the power input voltage is in the normal operating range as discussed for claim 5 (e.g., no power failure detected)]." EX1003, ¶¶457-461.

Ground 2: Ground 1 and Battery Backup of Amidi

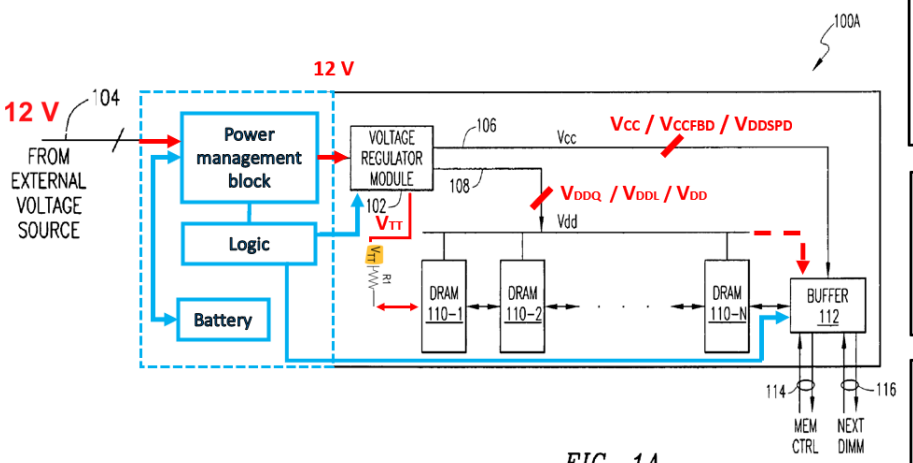


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

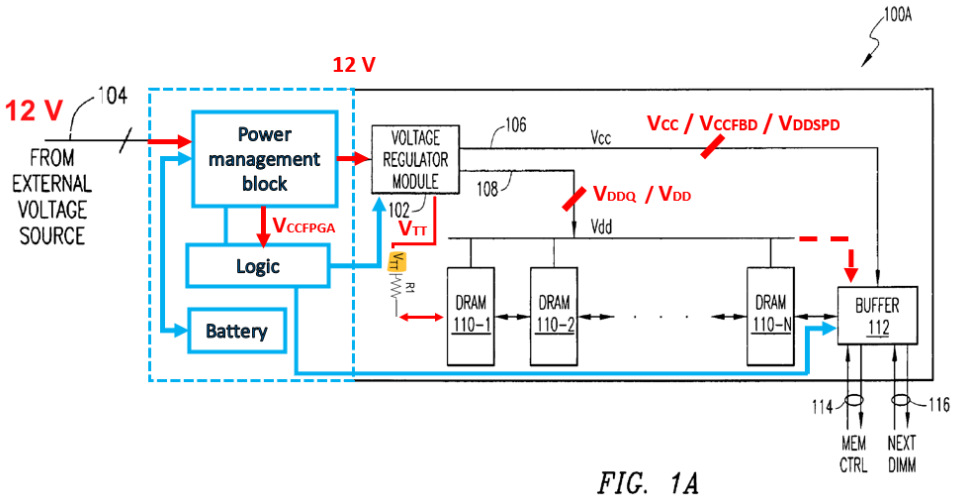


FIG. 1A

Voltage Mapping (D)
1st : VTT = 1.25V
2nd : VDD / VDDQ = 2.5V
3rd : VCCFPGA = 1.2V
4th : VDDSPD = 3.3V

13. Claims 16-22, 24-30

Claims 16 and 30 add a new limitation, "*pre-regulated input voltage*," discussed below (pp.73-75), but otherwise Grounds 2A-2D render obvious claims 16-19 and 21-22, and Grounds 2A-2C render obvious claims 20 and 24-30, for at least the same reasons discussed above, because these claims have limitations substantially identical to earlier limitations, as shown in the following table:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[16.a]	[1.a]	¶¶478-480 (¶¶216-222)
[16.b]	[1.b]	¶¶481-483 (¶¶223-231)
[16.c]	[1.c]-[1.e][4]	¶¶484-490 (¶¶232-280)
[16.d.1]	[1.f], [16.c]	¶¶491-493 (¶¶281-287, 484-490)
[16.d.2]	[1.c]-[1.f]	¶¶494-496 (¶¶232-287)
[16.e]	[1.g]-[1.h]	¶¶497-499 (¶¶288-303)
[16.f]	[5.a]-[5.b][5]	¶¶500-503 (¶¶360-376)
[17]	[2][6]	¶¶504-510 (¶¶328-347)
[18.a]	[16.a]	¶¶512-514 (¶¶478-480)
[18.b]	[12.c]	¶¶515-518 (¶¶453-456)

[4] With respect to "*pre-regulated input voltage*" in [16.c], see pp.73-75.

[5] The "*power input voltage received via a second portion of the plurality of edge connections*" in [5.b] corresponds to the "*input voltage received via a first portion of the plurality of edge connections*" in [16.f].

[6] Claims 2 and 17 both require two buck converters that "*are configured to operate as a dual buck converter*." Claim 2 recites the "*first and third buck converters*," while claim 17 recites "*the second and third buck converters*," but the invalidity arguments are similar either way. EX1003, ¶¶504-510.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[19]	[12.c]	¶¶519-523 (¶¶453-456)
[20]	[1.h], [3]	¶¶524-528 (¶¶298-303, 348-353)
[21.a]	[16.a]	¶¶530-532 (¶¶478-480)
[21.b.1]	[1.i.1]	¶¶533-536 (¶¶304-310)
[21.b.2]	[1.i.2][7]	¶¶537-540 (¶¶311-317)
[21.b.3]	[1.i.3]	¶¶541-544 (¶¶318-323)
[21.b.4]	[1.i.4]	¶¶545-548 (¶¶324-327)
[22.a]	[16.a]	¶¶550-552 (¶¶478-480)
[22.b]	[10.b], [15.b][8]	¶¶553-556 (¶¶432-438, 472-476)

[7] In [1.i.2], "*a first plurality of address and control signals via the first portion of the plurality of edge connections*" corresponds to "*a first plurality of address and control signals via a second portion of the plurality of edge connections*" in [21.b.2].

[8] In [22.b], "*the configuration information* [e.g., S3 configuration information stored in the non-volatile memory in the logic element as discussed in [10.b] and [15.b]] *is used to program the logic element*" because the S3 Configuration Registers are programmed and used to restore state when exiting S3 sleep mode. EX1003, ¶556; EX1027, pp.25, 39, 141.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[24.a]	[23.a]	¶¶599-600 (¶¶558-561)
[24.b]	[5.b]	¶¶601-604 (¶¶363-376)
[25.a]	[24.a]	¶¶606-608 (¶¶599-600)
[25.b]	[12.c]	¶¶609-613 (¶¶453-456)
[26]	[12.c]	¶¶614-618 (¶¶453-456)
[27]	[6]	¶¶619-623 (¶¶377-384)
[28]	[17]	¶¶624-628 (¶¶504-0)
[29]	[20]	¶¶629-633 (¶¶524-528)
[30]	[1.c]-[1.f], [13], [16.c]-[16.d.1]	¶¶634-638 (¶¶232-287, 457-461, 484-493)

For [16.c] and 30, to the extent a "*pre-regulated input voltage*" can be satisfied by the "*input voltage*" of [16.f] being within pre-determined limits, as suggested by Netlist, EX1071, p.43; EX1073, pp.49-50, Harris teaches that by disclosing an input voltage of 12 volts "+/- 15%" which can be "regulated." EX1023, ¶¶[0013-14]; EX1003, ¶¶487-488. To the extent the "*pre-regulated input voltage*" must be a voltage pre-regulated on the memory board itself, EX1001, 28:53-58, Amidi (in the combination for Ground 2) teaches a boost converter in the "power management block" that converts (and thus pre-regulates) the battery voltage to an output of 12 volts, as shown in the annotated figures below and as

discussed above (pp.52-56). EX1003, ¶489; EX1032, p.161 (explaining that switch-mode converters, including boost converters, "convert the ***unregulated*** dc input into a ***controlled*** dc output at a desired voltage level"). Furthermore, it would have been obvious to include a power regulator in the "power management block" that ensures a pre-regulated output voltage of 12V given Harris's teaching that the external supply voltage may be "unregulated," EX1012, ¶[0014], and to allow compatibility with external supply voltages other than 12V, EX1023, ¶[0020]; EX1032, p.161. EX1003, ¶489.

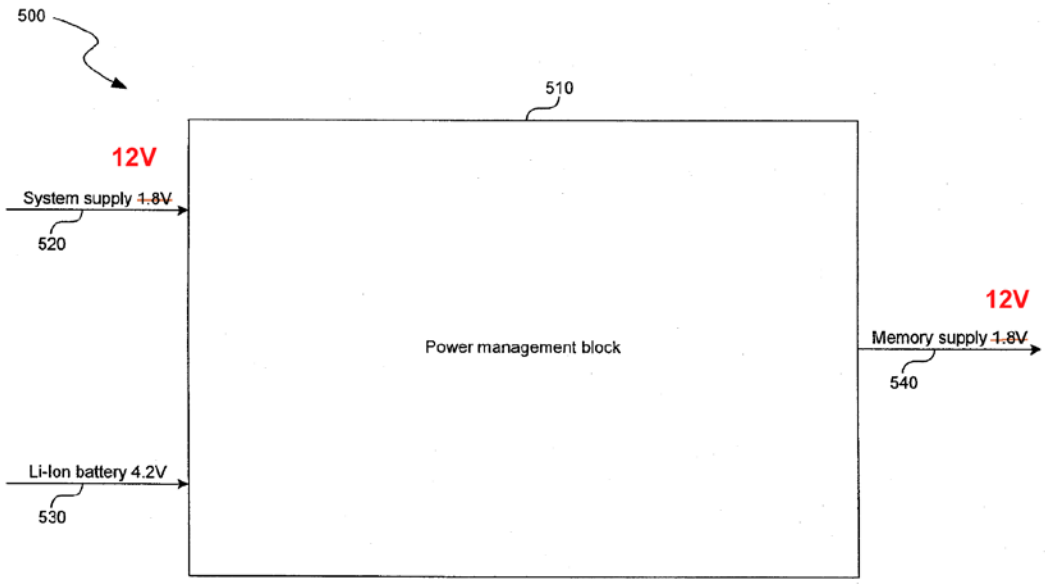


FIG. 5

Ground 2: Ground 1 and Battery Backup of Amidi

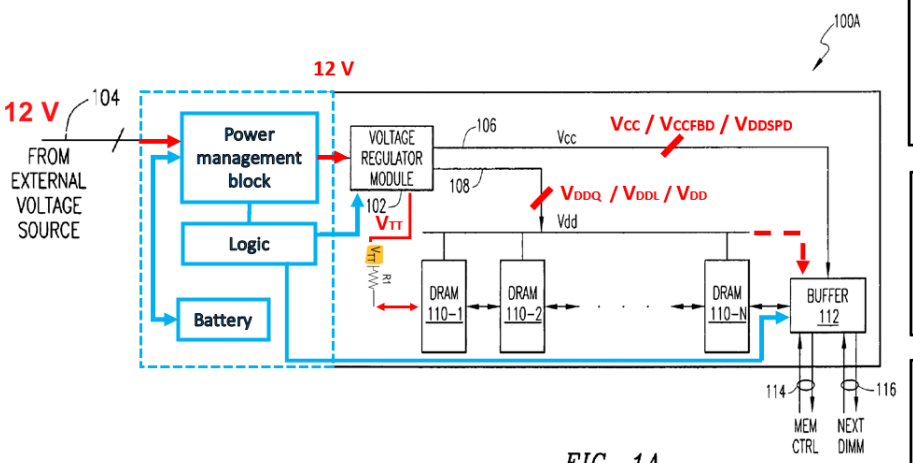


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

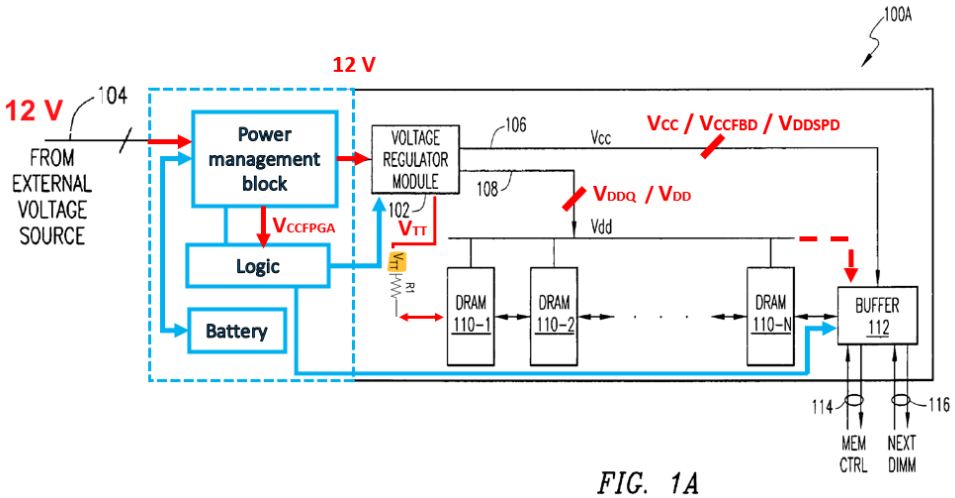


FIG. 1A

Voltage Mapping (D)
1st : VTT = 1.25V
2nd : VDD / VDDQ = 2.5V
3rd : VCCFPGA = 1.2V
4th : VDDSPD = 3.3V

C. Ground 3

Ground 3 renders obvious claims 1-30.

1. Ground 3 combination: Ground 2 + Hajeck (EX1038)

Ground 3 combines Ground 2 with the teachings of Hajeck, which discloses a "voltage detection circuit 48" for detecting both undervoltage and overvoltage anomalies in memory subsystems. EX1038, 3:30-40, Fig.1; EX1003, ¶¶180-187.

Hajeck is analogous art to Harris and Amidi in Ground 2 as all relate to memory subsystems in general and protecting against power disruptions in particular. EX1003, ¶182. A POSITA would have been motivated to combine Ground 2 with Hajeck, and had a reasonable expectation of success in doing so, because Amidi discloses providing battery backup upon detecting undervoltage anomalies, EX1024, 4:44-53, and Harris teaches the need to detect both undervoltage and overvoltage anomalies beyond a "15%" threshold, EX1023, ¶[0013], and Hajeck teaches how to detect both undervoltage and overvoltage anomalies to avoid data loss, EX1038, 1:10-31, 3:30-40, 4:62-65, consistent with techniques that were already well-known, *see, e.g.*, EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5; EX1063, pp.1-2; EX1061, p.15; EX1062, p.15. Thus, a POSITA would have looked to Hajeck's teachings related to overvoltage anomalies when implementing Amidi's voltage supervisory block in Ground 2 so that it detects both undervoltage and overvoltage anomalies. EX1003, ¶¶185-187.

The teachings of Hajeck do not affect any of the voltage mappings in Ground 2, and thus the voltage mappings for Grounds 3A-3D are the same as those for Grounds 2A-2D above (pp.27, 60, 55-56).

2. Claims 1-30

Ground 3 renders obvious claims 1-30 for at least the same reasons provided above for Ground 2 (pp.56-75). To the extent one were to argue that Ground 2

fails to teach overvoltage protection as required by [5.b] ("*the power input voltage having an amplitude that is greater than a first threshold voltage*") and as discussed above (pp.60-63) — and required by claims 6-7, 9-13, [16.f], 17-22, 24-27 — such overvoltage protection was obvious in light of Hajeck in the combination for Ground 3. EX1003, ¶¶375-376. As explained above for the combination of Ground 3 (pp.75-76), a POSITA would have looked to Hajeck's teachings about overvoltage anomalies when implementing Amidi's voltage supervisory block to detect both undervoltage and overvoltage anomalies. EX1003, ¶¶185-187. In particular, in the combination for Ground 3, Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (EX1024, 4:44-52), but also "when the voltage exceeds a certain level" as taught by Hajeck (EX1038, 3:30-43; *see also id.* Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, Fig. 1). Thus, Ground 3 further teaches both overvoltage and undervoltage detection and protection, further rendering obvious claims 5, 16, 24, and their dependents (6-7, 9-13, 17-22, and 25-27). EX1003, ¶¶375-376, 383-384, 425, 503, 604.

D. Ground 4

Ground 4 renders obvious claims 1-30.

1. Ground 4 combination: Spiers (EX1025) + Amidi (EX1024)

Ground 4 is based on Spiers in view of Amidi, implemented with DDR2 or DDR3 SDRAMs as follows:

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

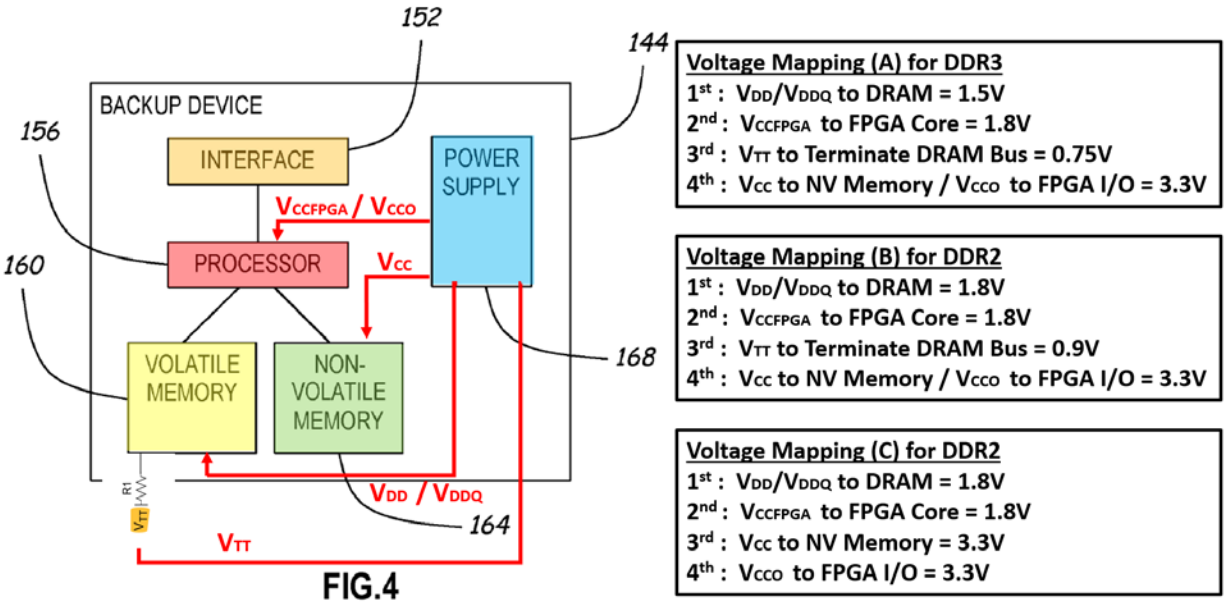


FIG.4

EX1003, ¶¶188-206; EX1025, Fig.4.

Spiers is remarkably similar to the 918 Patent: in the event of a power disruption, both teach transferring data from the volatile (SDRAM) memory (yellow) to the non-volatile (NAND flash) memory (green), as discussed previously (pp.5-7, 13-14). Amidi is analogous art that is similarly directed to providing backup capabilities to memory modules in the event of power disruptions, as discussed above (pp.12-12). A POSITA would have been motivated to consult Amidi's disclosure when implementing Spiers to learn

specific implementation details, such as specific type of SDRAM devices and voltage regulators. EX1003, ¶¶196-200.

For example, Spiers teaches using volatile SDRAM devices in general, EX1025, ¶[0010], Fig.5 (190), while Amidi specifically discloses DDR SDRAM devices, EX1024, claims 4-5. A POSITA would have been familiar with the JEDEC standards for DDR2 (EX1026) and DDR3 (EX1046) SDRAMs, which specify particular voltages required for those memory devices. EX1003, ¶¶198-200. Indeed, DDR SDRAM (like NAND flash) was "off-the-shelf…commercially available." EX1064, ¶¶[0032, 29, 36-37]. Thus, a POSITA would have been motivated to implement Spiers with DDR2 or DDR3 SDRAMs powered according to the relevant standards, and had a reasonable expectation of success when using such well-known, standardized technology. EX1003, ¶¶198-200.

Ground 4, as summarized in the annotated figure above (p.78), includes DDR2 or DDR3 SDRAMs with the standard voltages below, and thus a POSITA would have been motivated to implement Spiers's Power Supply (168 above, blue) to supply these voltages. EX1003, ¶¶200-206.

- DDR3:
  - 1.5V for **V_{DD}/V_{DDQ}** to DDR3 SDRAM (160, yellow). EX1046, p.10:

V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage

- 0.75V for **V_{TT}** to resistors and DDR3 SDRAM. *Id.*, p.109 ("$V_{TT}=V_{DDQ}/2$").

- DDR2:
  - 1.8V for **V_{DD}/V_{DDQ}** to DDR2 SDRAM (160, yellow). EX1026, pp.6-7:

V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

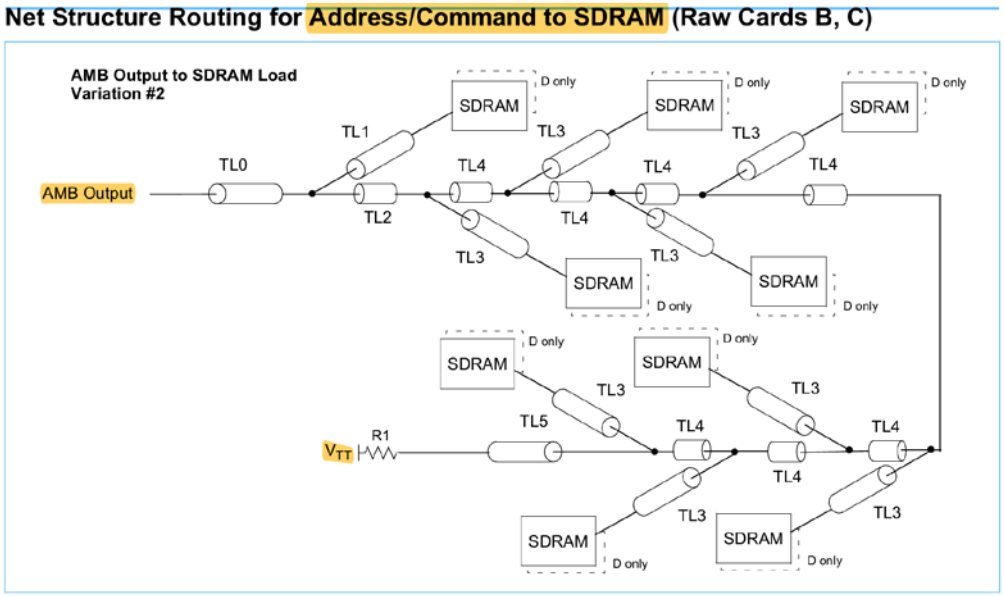
  - 0.9V for **V_{TT}** to resistors and DDR2 SDRAM. *Id.*, p.71 ("$V_{TT}=V_{DDQ}/2$").

- 3.3V for **V_{CC}** to non-volatile memory (164, green). EX1025, ¶[0037], Fig.5 (184, "3.3V"); EX1049, p.38.

- 3.3V for **V_{CCO}** to input/output of the Processor (156, red), which could be implemented using an FPGA according to Spiers. *Id.*; EX1042, pp.2, 16.

- 1.8V for V_{CCFPGA} to the core of the Processor (156, red). EX1025, ¶[0037], Fig.5 (206, "1.8V"); EX1042, pp.2, 16 (labeled V_{CCINT}).

See also EX1028, p.68:



In the annotated figure for Ground 4 above (p.78), Voltage Mappings "A" to "C" (on the right) are simply different ways to apply the arbitrary labels "1st" through "4th" to the voltages shown in red in the annotated figure. EX1003, ¶¶201-206.

Below, Ground 4A refers to Ground 4 above with Voltage Mapping "A," while Grounds 4B and 4C refer to Ground 4 above with Voltage Mappings "B" and "C," respectively. *Id.*

2. Independent Claim 1

a) [1.a] Preamble

To the extent the preamble is limiting, Grounds 4A-4C teach "*[a] memory module comprising* [e.g., Spiers's backup device 144 (below) implemented in a PCI card including volatile memory (SDRAMs 190, yellow) and non-volatile memory (NAND Flash 194, green), and configured to store data in a memory system]." EX1003, ¶¶643-646; EX1025, ¶¶[0034, 37], Figs. 3, 5.

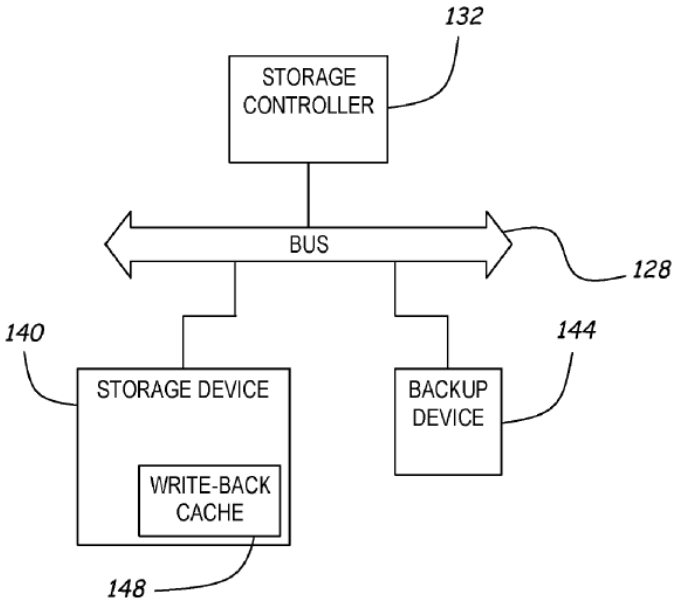
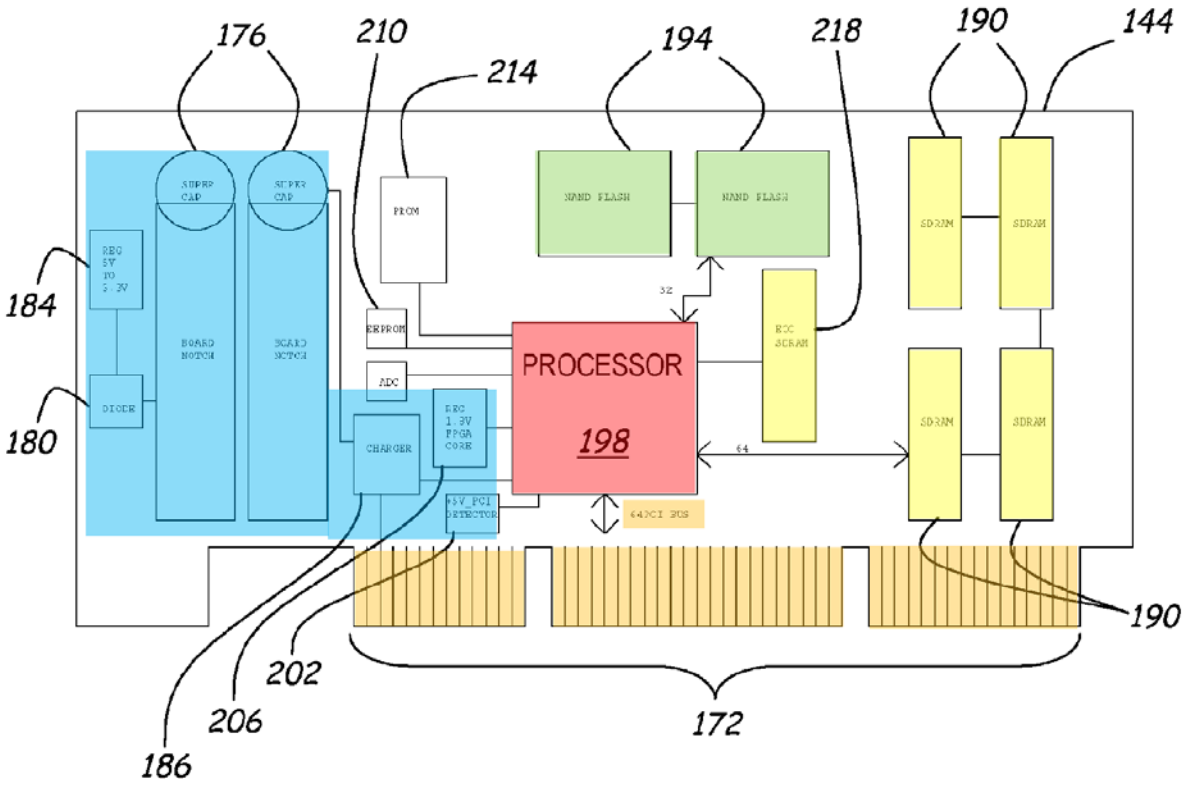


FIG.3



b) [1.b] Printed Circuit Board (PCB)

Grounds 4A-4C teach "*a printed circuit board (PCB)* [PCI card of backup device 144, above] *having an interface* [64-bit PCI card connector 172, orange above] *configured to fit into a corresponding slot connector of a host system* [e.g., "5 volt" PCI Board Connector, below], *the interface including a plurality of edge connections* [orange above]." EX1003, ¶¶647-654; EX1025, Fig.5 (above); EX1031 (PCI standard), pp.114 (below), 152, 298.

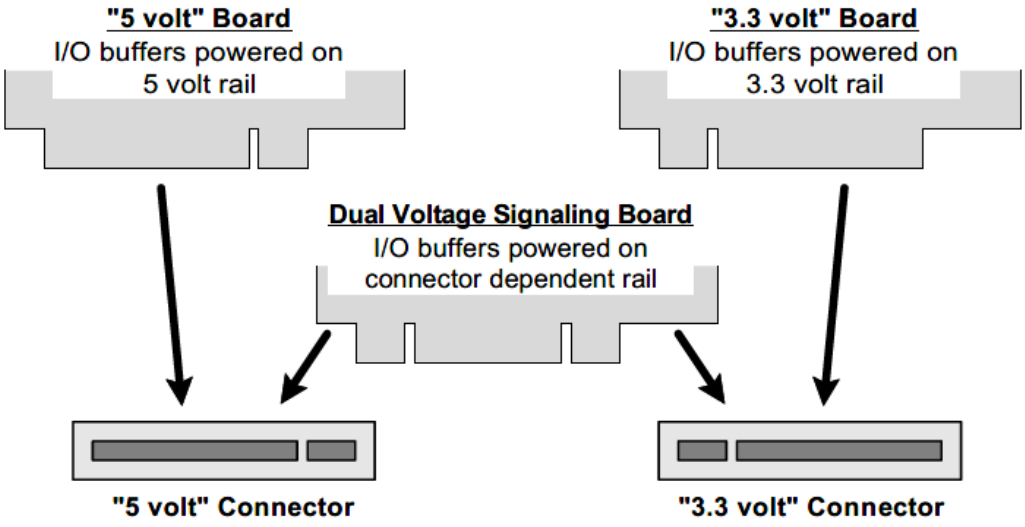


Figure 4-1: PCI Board Connectors

Grounds 4A-4C also teach that the "*edge connections*" are "*configured to couple power, data, address and control signals between the memory module and the host system*": The PCI connector 172 has "*edge connections configured to couple power,*" including a +5V power supply monitored by +5V PCI detector 202. EX1003, ¶651; EX1025, ¶¶[0037, 54]; EX1031, pp.146-50. The "64-bit PCI bus" "*edge connections*" of connector 172 also couple "*data, address and control signals*" with read or write commands from the host. EX1003, ¶¶652-654; EX1025, ¶¶[0037, 39], Figs. 9-11; EX1031, pp.1, 7 (Fig. 2-1, below), 10, 21-25 (below).

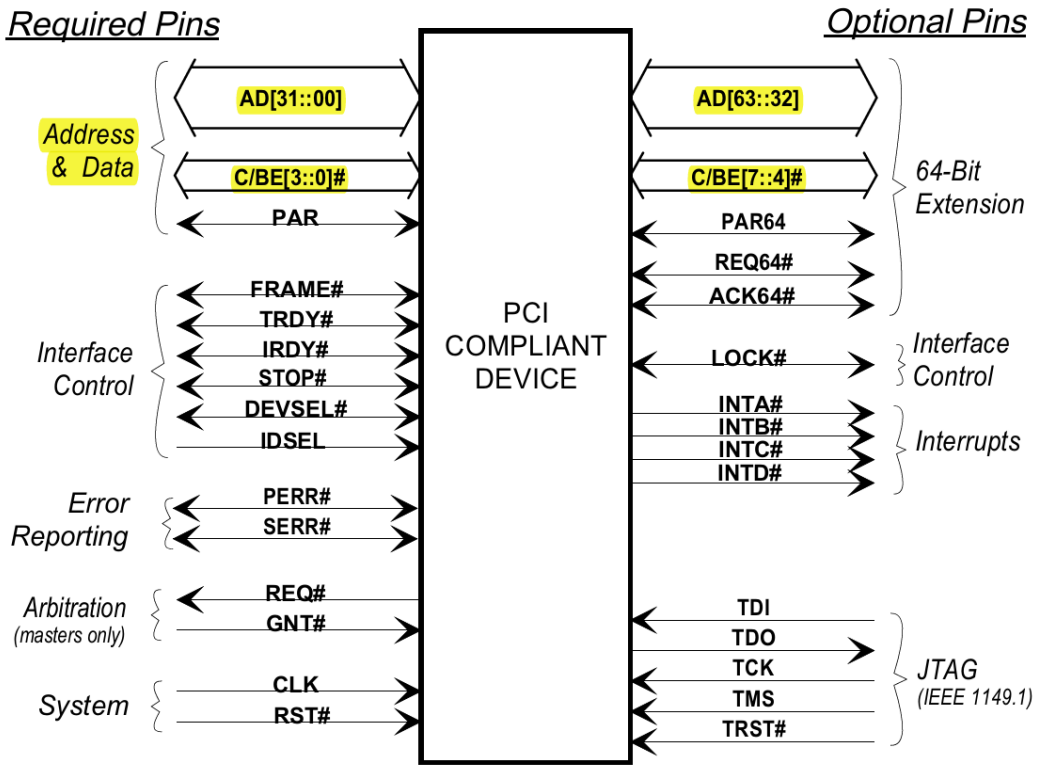


Figure 2-1: PCI Pin List

3.1.1. Command Definition

PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

c) [1.c] to [1.f] First to Fourth Regulated Voltages

Grounds 4A-4C teach "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude* ["1st"/"*first*" below]*; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude* ["2nd"/"*second*" below]*; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude* ["3rd"/"*third*" below]*; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude* ["4th"/"*fourth*" below]," when backup device 144 is implemented with DDR3 or DDR2 DRAMs as shown in Voltage Mappings A and B-C, respectively, below:

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

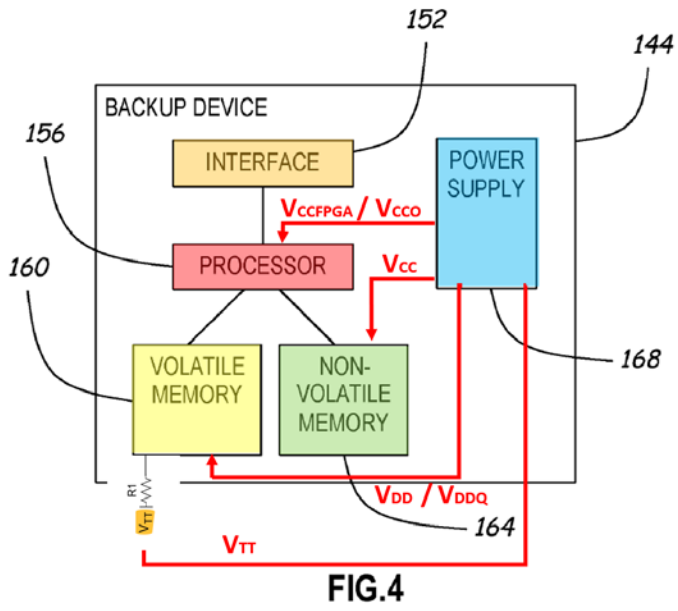


FIG.4

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.75V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.9V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VCC to NV Memory = 3.3V
4th : VCCO to FPGA I/O = 3.3V

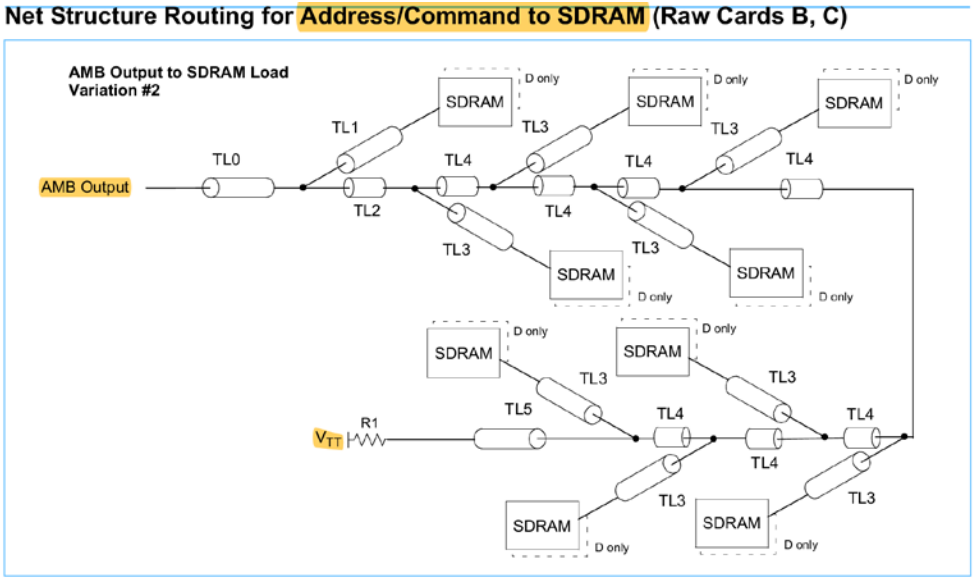
See supra pp.78-81; EX1003, ¶¶655-700.

	Voltage Mappings (Grounds 4-5)		
	A	B	C
"*first*":	V_{DD}/V_{DDQ}=1.5V	V_{DD}/V_{DDQ}=1.8V	V_{DD}/V_{DDQ}=1.8V
"*second*":	V_{CCFPGA}=1.8V	V_{CCFPGA}=1.8V	V_{CCFPGA}=1.8V
"*third*":	V_{TT}=0.75V	V_{TT}=0.9V	V_{CC}=3.3V
"*fourth*":	V_{CC} or V_{CCO} = 3.3V	V_{CC} or V_{CCO} = 3.3V	V_{CCO}=3.3V

Id. Grounds 4B-4C have "*voltage amplitude[s]*" that are the same, consistent with Netlist's broad interpretation of the claim, EX1071, p.43; EX1073, pp.49-53, while Ground 4A does not, consistent with a narrower interpretation. Furthermore, given that Grounds 4A-4C disclose a range of voltages, any specific voltage combinations within that range are obvious under Federal Circuit precedent discussed above (p.27).

Spiers discloses that the PCI card monitors and uses the "+5 volt" power supply of the PCI bus to power components of the card, including the SDRAM devices (190, 218) requiring power supply voltages, such as V_{DD}/V_{DDQ} ("*first regulated voltage*") with amplitudes depending on the specific SDRAM type (DDR2, DDR3, etc.) as discussed above (pp.79-81). EX1003, ¶¶655-661, ¶¶693-694; EX1025, ¶¶[0037, 54], Figs. 5, 14. A POSITA would have also recognized that a V_{TT} termination voltage ("*third regulated voltage*" in mappings A and B), whose amplitude is half of V_{DD}/V_{DDQ} as discussed above (pp.79-81), is also

required for communicating with the DRAM devices, just like in an FBDIMM design. EX1003, ¶¶680-684; EX1025 Fig. 9, ¶¶[0037, 46]; EX1028, p.68 (below).



Spiers further discloses a voltage regulator 206 which provides V_{CCFPGA}=1.8V regulated power to the FPGA core ("*second regulated voltage*"). EX1003, ¶¶670-673; EX1025, ¶[0037], Fig. 5 (below, left). A POSITA would have also understood that different FPGAs had different voltage requirements for the FPGA core. EX1042, p.2 (labeled V_{CCINT} below, right).

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

Spiers also discloses a voltage regulator 184 configured to step down a 5V backup voltage to a 3.3V output voltage which is used to transfer the data from the volatile to the non-volatile memories 194. EX1003, ¶¶685-687, 691-698; EX1025,

Fig. 5 (below, left). A POSITA would have understood that 3.3V can be used as V_{CC} power to the non-volatile memories ("*third regulated voltage*" in Mapping C, "*fourth regulated voltage*" in Mappings A and B). *Id*., EX1049, p.38 (below, right).

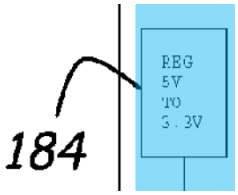
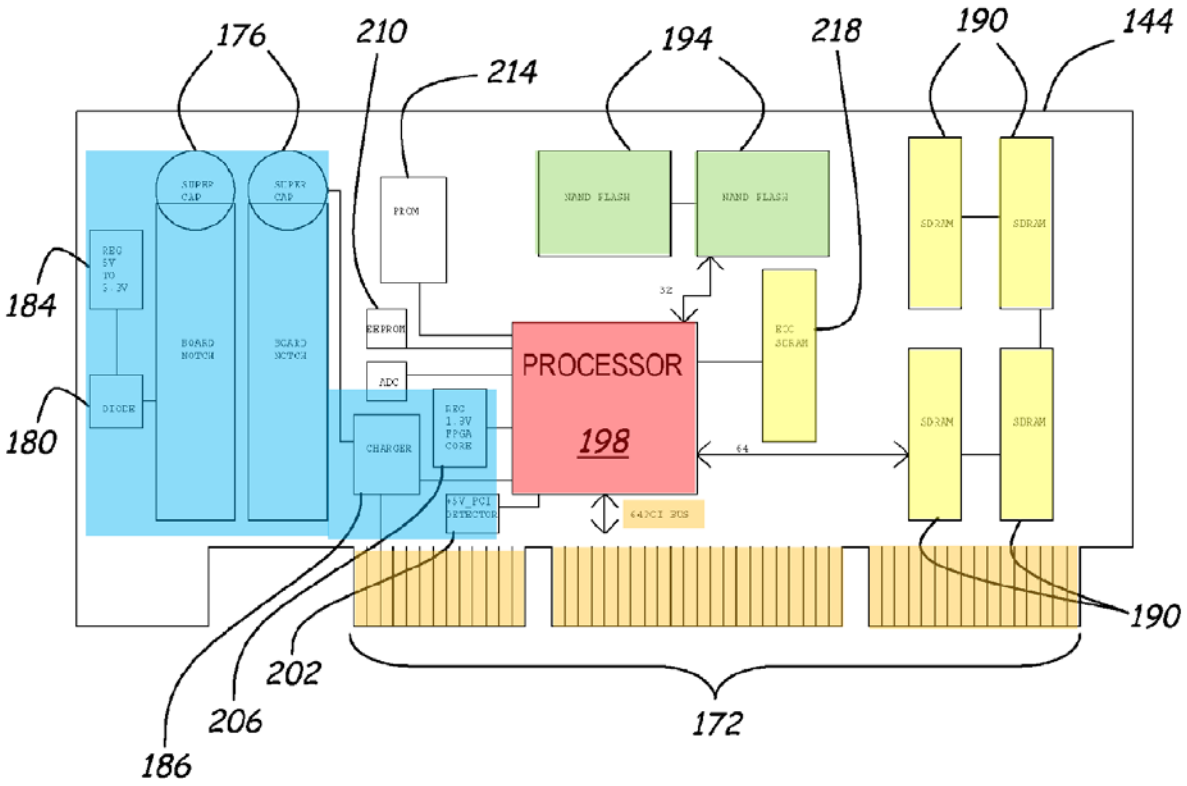


Table 12: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	^{t}A	0	–	+70	°C
	Extended	^{t}A	–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Supply voltage		Vss	0	0	0	V

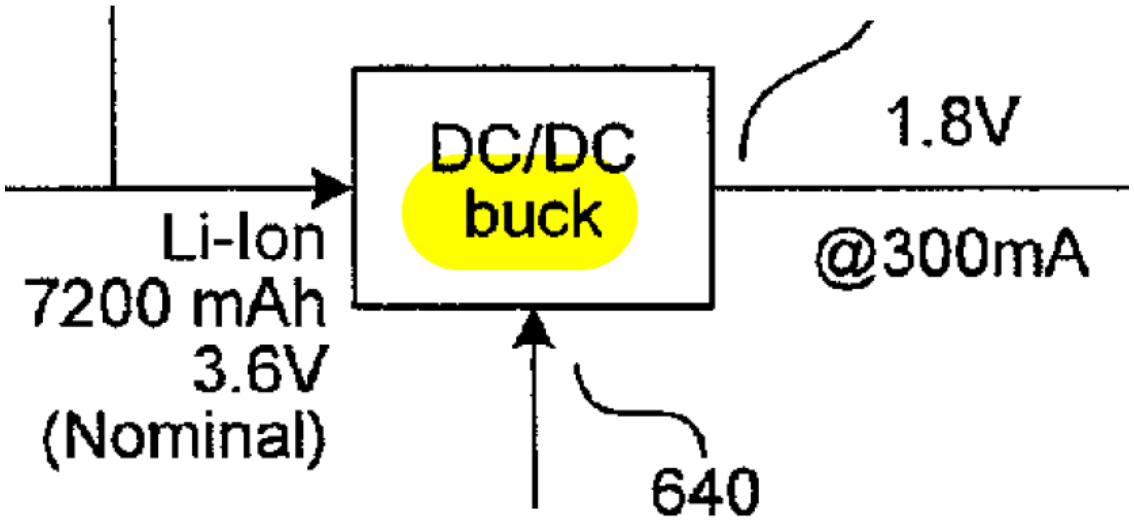
A POSITA would have also understood that a converter circuit, such as voltage regulator 184 or another, similar voltage converter, is configured to provide a regulated voltage V_{CCO} of 3.3V ("*fourth regulated voltage*" in mapping C, "*third regulated voltage*" in mappings A and B) to an interface of the processor 198 (red) to transfer data to and from the non-volatile memories 194 (green). EX1003, ¶¶691-700; EX1042, pp.2, 16 (V_{CCO}).



Furthermore, it would have been obvious to a POSITA to use "*buck converter[s]*" to provide each[9] of these regulated voltages from the +5V power supply in order to achieve high efficiency, reliability, and flexible power conversion, as discussed previously (pp.29-31). EX1003, ¶¶662-666. Indeed, any loss at the power conversion creates heat that needs to be removed by additional cooling and takes away time from Spiers's backup operation, risking its successful completion. *Id.*; EX1025, Fig. 14 (step 752); EX1062, p.11 ("lower dissipation … saves the cost (and space) of cooling apparatus").

[9] See note 2 on p.28.

Buck converters powering SDRAM and FPGA devices from higher voltage sources were well known and commercially available at the time, as disclosed by Amidi (below, part of the combination in Ground 4) and others. EX1003, ¶¶663-665, 673-674.



EX1024 (Amidi), Fig. 6 (640), 4:38-41; *see also* EX1047, 1:28-32, 2:47-55, 5:56-59, 7:6-14; EX1041, pp.1-2, 9 (first below); EX1042, p.16 (second below); EX1048, pp.1-2 (third below); EX1058, p.5 (fourth below).

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

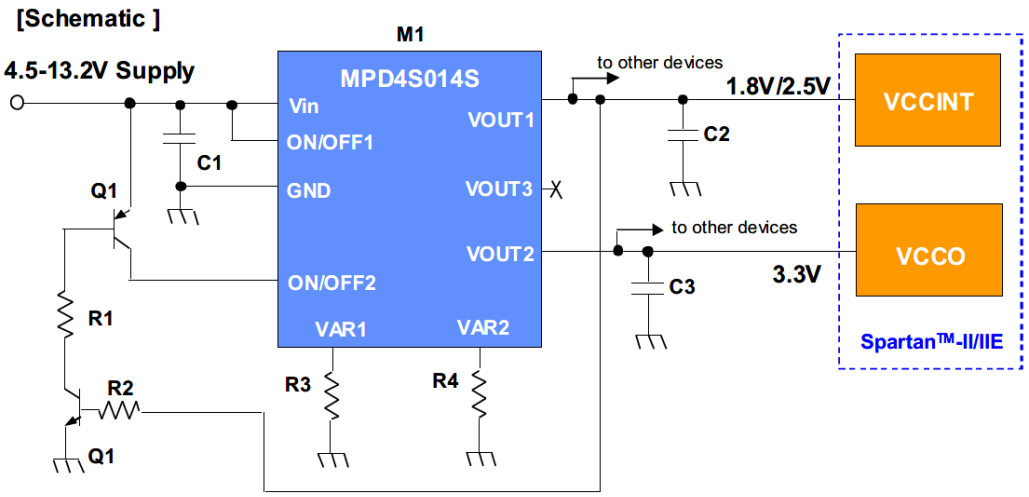
Applications

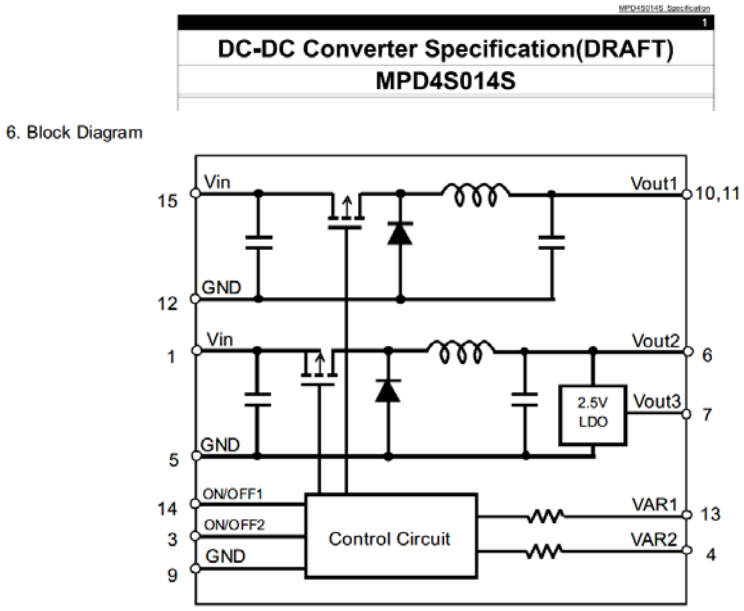
- DDR V_{DDQ} and V_{TT} voltage generation

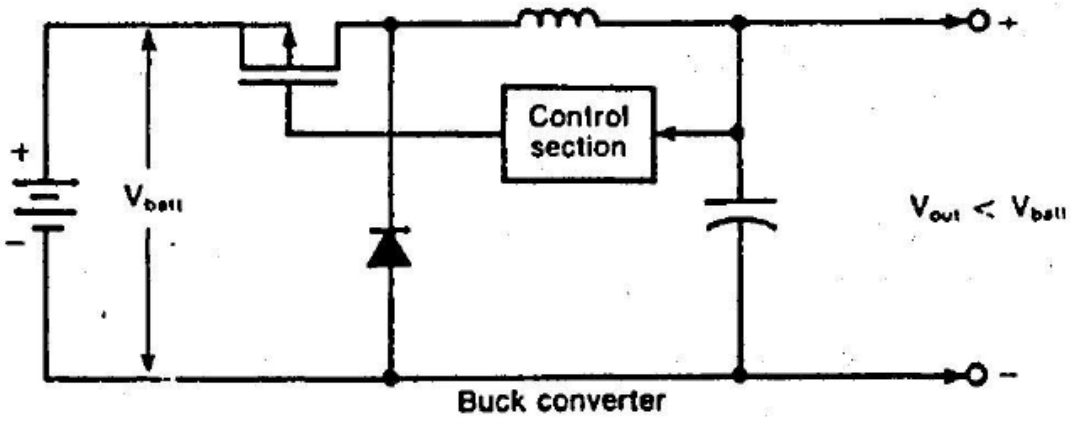
Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.


[Schematic]
M1
4.5-13.2V Supply
MPD4S014S
Vin
ON/OFF1
GND
ON/OFF2
VAR1
VAR2
VOUT1
VOUT3
VOUT2
to other devices
1.8V/2.5V
C1
C2
C3
Q1
R1
R2
R3
R4
Q1
to other devices
3.3V
VCCINT
VCCO
Spartan™-II/IIE


DC-DC Converter Specification(DRAFT)
MPD4S014S
6. Block Diagram
Vin
GND
Vin
GND
ON/OFF1
ON/OFF2
GND
Control Circuit
Vout1
Vout2
2.5V LDO
Vout3
VAR1
VAR2
15
12
1
5
14
3
9
10,11
6
7
13
4


Control section
V_{batt}
$V_{out} < V_{batt}$
Buck converter

d) [1.g] A Plurality of Components Coupled to the PCB

Grounds 4A-4C teach "*a plurality of components* [e.g., DRAM, FPGA/Processor, resistors, and non-volatile memory, as discussed above (pp.78-81) and shown below] *coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages* [as discussed above (pp.78-81) and shown below]." EX1003, ¶¶701-713.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

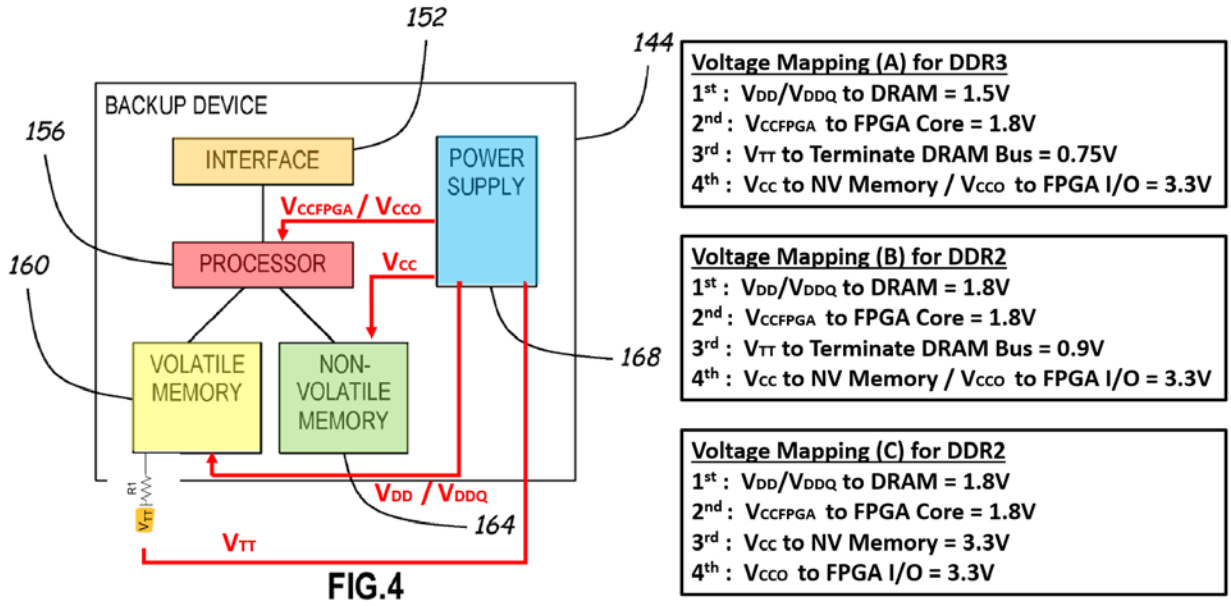


FIG.4

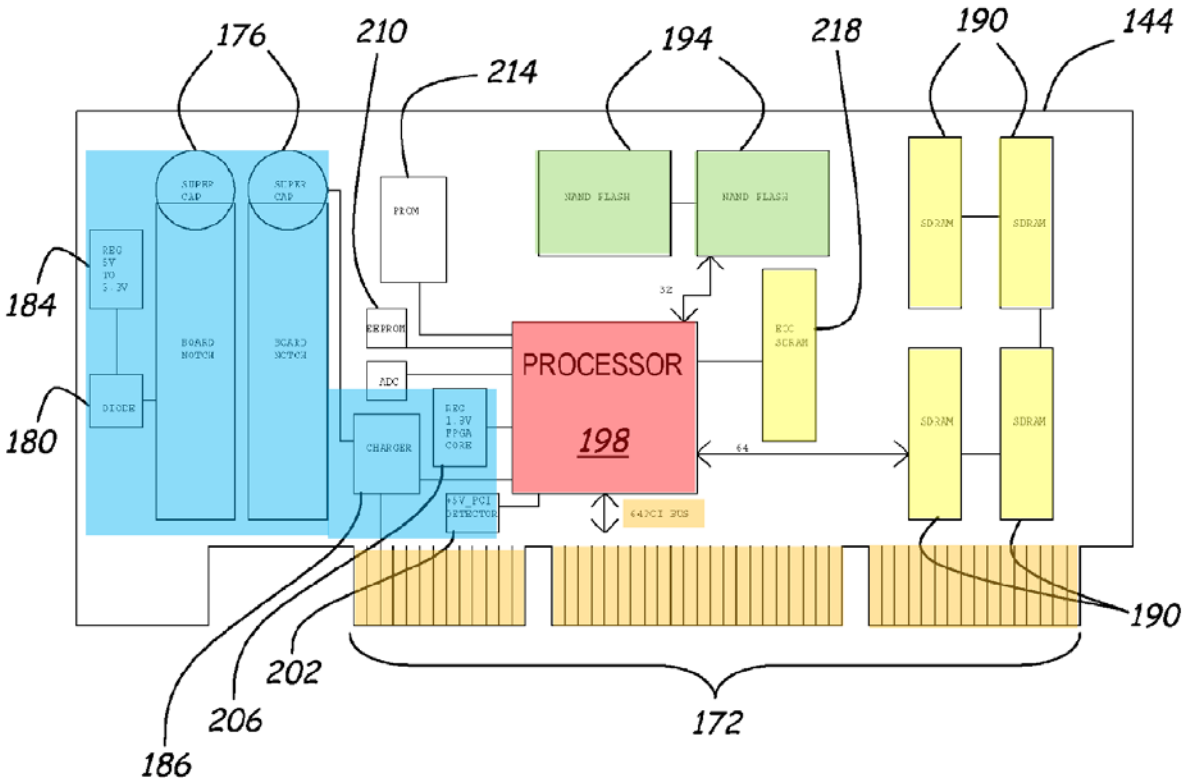
e) [1.h] A plurality of SDRAM devices coupled to the first regulated voltage

Grounds 4A-4C teach "*a plurality of synchronous dynamic random access memory (SDRAM) devices* [e.g., 190, yellow below, implemented as DDR2 or DDR3] *coupled to the first regulated voltage*" as discussed above (pp.78-81, 32). EX1003, ¶¶714-718.

f) [1.i.] At least one circuit

(1) [1.i.1] Coupled between edge connection and SDRAM devices

Grounds 4A-4C teach "*at least one circuit* [FPGA processor 198 (red)] *coupled between a first portion of the plurality of edge connections* [PCI interface 172 (orange), e.g., for address and control [from [1.b]] *and the plurality of SDRAM devices* [190, 218 (yellow)]." EX1003, ¶¶719-723; EX1025, Fig. 5 (below), ¶[0037].



(2) [1.i.2] Operable to receive/output address and control signals

Grounds 4A-4C teach that "*the at least one circuit* [FPGA processor 198 (red, above) is] *operable to (i) receive a first plurality of address and control*

signals [below, for read and write commands] *via the first portion of the plurality of edge connections* [in PCI interface 172 (orange, above)], *and (ii) output a second plurality of address and control signals* [on DDR SDRAM interface between 198 and 190] *to the plurality of SDRAM devices* [190 (yellow, above)]" for the reasons discussed above for [1.b], plus those below. EX1003, ¶¶724-729; EX1025, ¶[0037], Fig.5 (above); EX1031, pp.1, 7 (Fig. 2-1, PCI interface, first below), 21 (PCI commands, second below), 146-49 (pin assignments for "AD" and "C/BE").

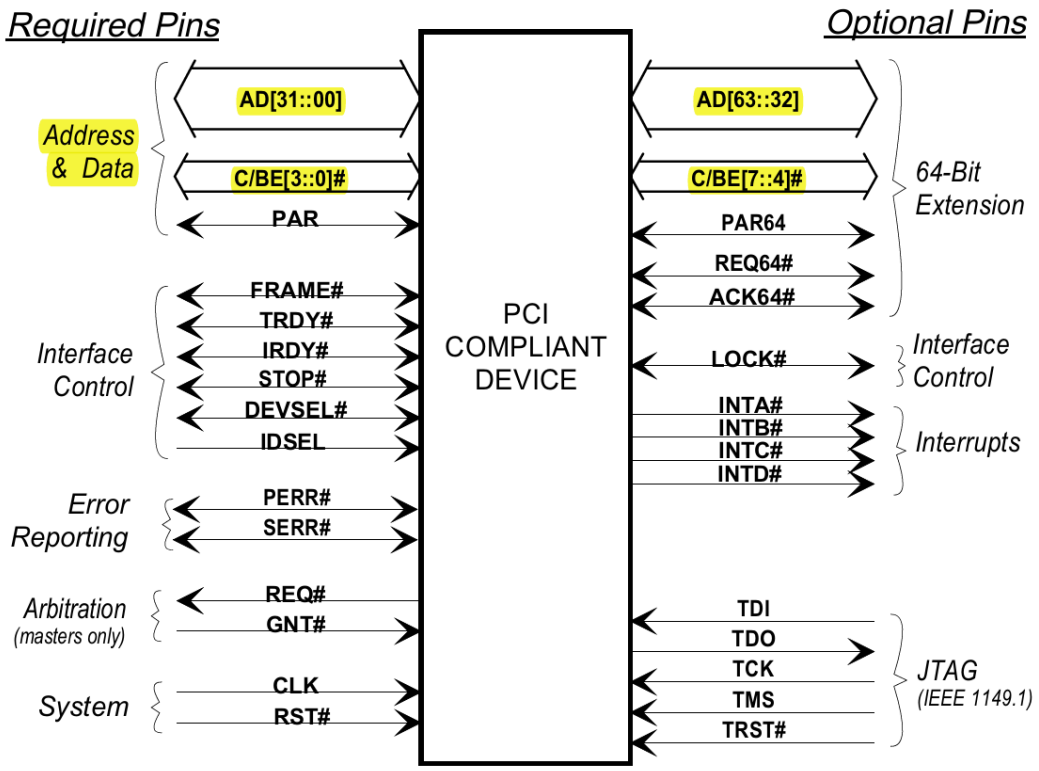


Figure 2-1: PCI Pin List

3.1.1. Command Definition

PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

For example, Spiers discloses the processor receiving read and write commands with respective addresses from the host, queuing them in a FIFO, decoding the received signals, and outputting address and control signals to the SDRAMs to read and write accordingly, as shown below. EX1003, ¶728; EX1025, Fig. 9 (below), ¶¶[0039, 44-46].

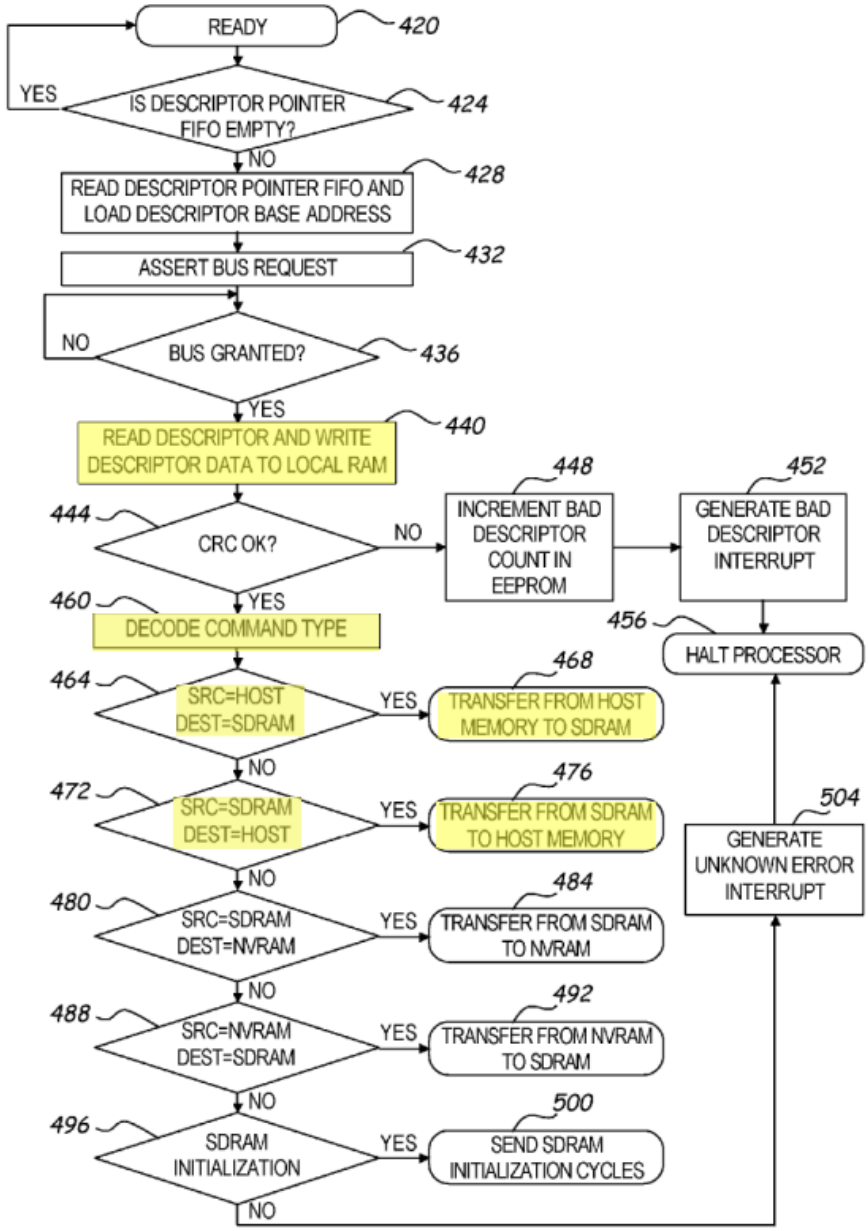


FIG.9

(3) [1.i.3] Coupled to both the second and fourth regulated voltage

Grounds 4A-4C teach "*the at least one circuit* [FPGA processor (red)] *coupled to both the second regulated voltage* [e.g., V_{CCFPGA}=1.8V] *and the fourth regulated voltage* [e.g., V_{CCO}=3.3V to interface with non-volatile memory]" as

shown below and discussed above (pp.78-81) and for [1.c]-[1.f]. EX1003, ¶¶730-734.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

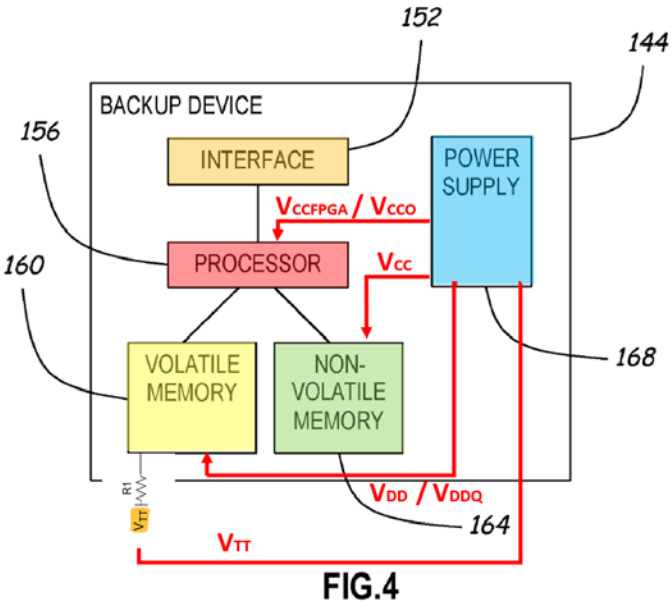


FIG.4

Voltage Mapping (A) for DDR3
1st : VDD/VDDQ to DRAM = 1.5V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.75V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VTT to Terminate DRAM Bus = 0.9V
4th : VCC to NV Memory / VCCO to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : VDD/VDDQ to DRAM = 1.8V
2nd : VCCFPGA to FPGA Core = 1.8V
3rd : VCC to NV Memory = 3.3V
4th : VCCO to FPGA I/O = 3.3V

(4) [1.i.4] Wherein the second and fourth regulated voltage amplitudes are different

Grounds 4A-4C teach "*wherein a first one of the second and fourth voltage amplitudes* [e.g., 1.8V] *is less than a second one of the second and fourth voltage amplitudes* [e.g., 3.3V]" as shown above (pp.78-81, 87). EX1003, ¶¶735-738.

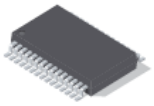
3. Claim 2

Grounds 4A-4C teach "*claim 1, wherein the first* [e.g., for V_{DD}/V_{DDQ} (pp.78-81)] *and third* [e.g., for V_{TT} or V_{CC} (pp.78-81)] *buck converters are further configured to operate as a dual buck converter* [e.g., to use fewer integrated circuits, pins, and interconnections on the module, consistent with commercially available dual buck converters such as EX1040, p.1 (below) and EX1041, pp.1-2

(below), 9 (showing two converters with different phases can reduce ripples), and, for voltage mappings A and B, to have V_{TT} follow the fluctuations of V_{DD}/V_{DDQ}, EX1040, p.11]." EX1003, ¶¶739-746.

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- **Notebook Computers System Bus and I/O**
- **DDR I or DDR II Termination**

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

- DDR V_{DDQ} and V_{TT} voltage generation

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Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

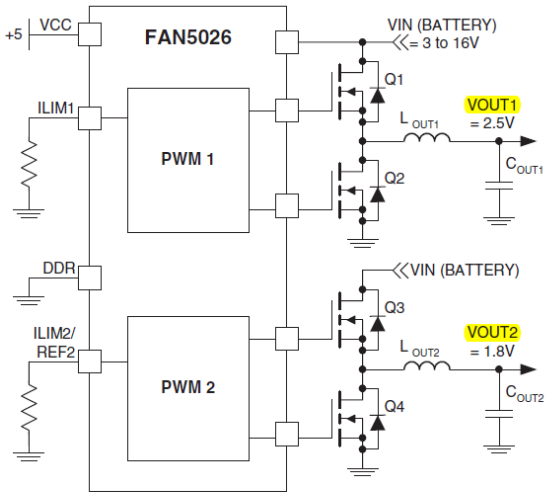


Figure 1. Dual Output Regulator

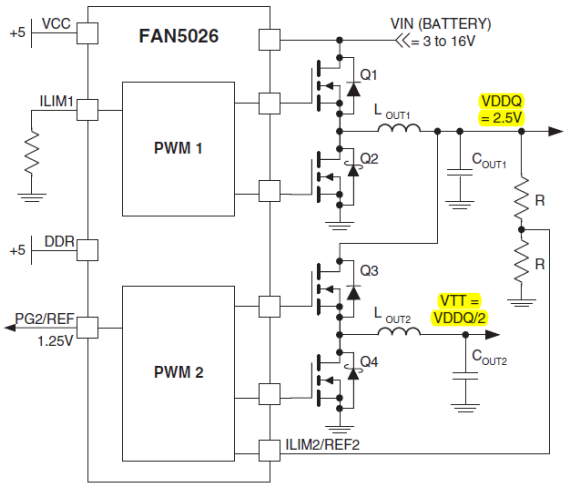


Figure 2. Typical Application

4. Claim 3

Grounds 4B-4C teach "*claim 1, wherein the first voltage amplitude is 1.8 volts*," as shown below and discussed above (pp.78-81, 87). EX1003, ¶¶747-751.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

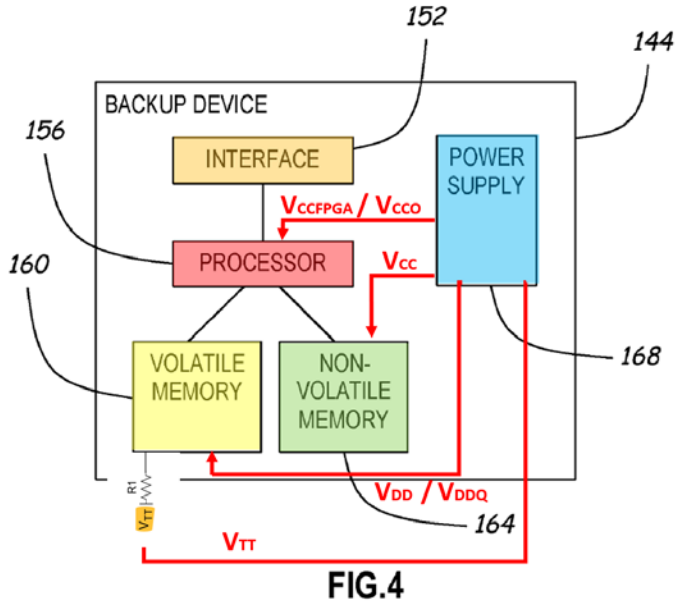


FIG.4

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.75V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.9V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

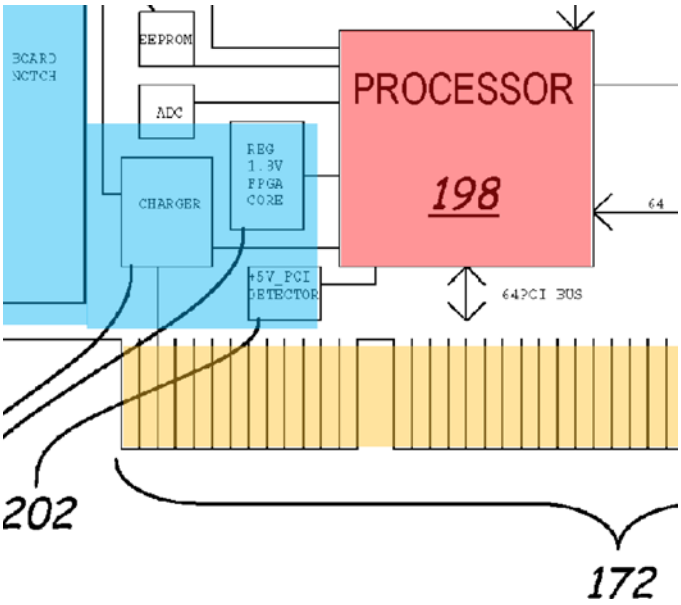
Voltage Mapping (C) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{CC} to NV Memory = 3.3V
4th : V_{CCO} to FPGA I/O = 3.3V

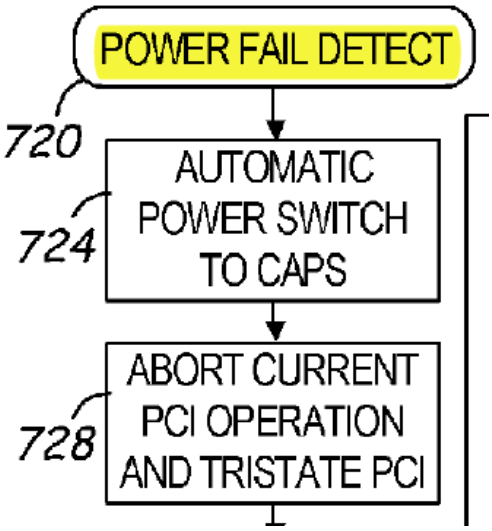
5. Claim 4

Claim 4 is "*claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively*." These claimed voltages fall within the range of voltages disclosed in the prior art as shown by Grounds 4A-4B, and thus they are obvious under Federal Circuit precedent discussed above (p.27). EX1003, ¶¶752-762.

6. Claim 5

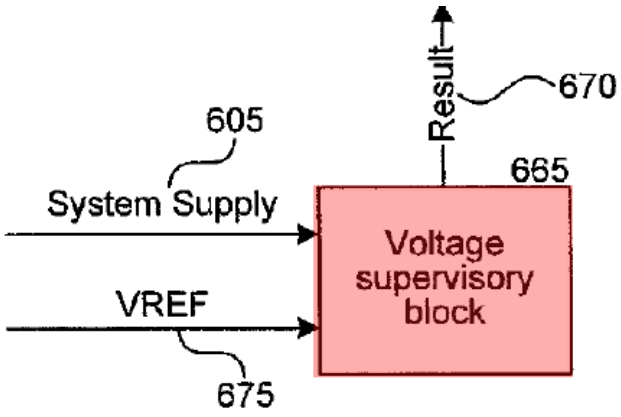
Grounds 4A-4C teach "*claim 1, further comprising: a voltage monitor circuit* [e.g., Spiers's +5V PCI detector 202 (blue, below)] *configured to monitor a power input voltage received via a second portion of the plurality of edge connections* [e.g., monitors the +5V PCI supply voltage received at a +5V pin of the PCI connector 172 (orange)], *the voltage monitor circuit configured to produce a trigger signal* [e.g., Spiers's signal from detector 202 (blue) to processor 198 (red) at step 720 (Fig.14)]…" EX1003, ¶¶763-778; EX1025, ¶¶[0036-37, 54], Figs. 5 (below, left), 14 (below, right).





Grounds 4A-4C also teach that the "*trigger signal*" from detector 202 is produced "*in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage* [e.g., overvoltage protection]," as explained below. EX1003, ¶¶770-778.

Amidi discloses the details of power failure detection, and thus in the combination for Ground 4 it would have been obvious to implement Spiers's detector 202 to compare the system supply (e.g., 605 below) to a reference (e.g., 675) ("*first threshold voltage*") to generate a trigger signal (e.g., 670) similar to Amidi's teachings. *See* EX1024, 4:44-52, 5:35-43, 8:23-29, 9:8-12, Figs. 5, 6 (excerpted, annotated below), 8, 14 (reproduced below), 15.



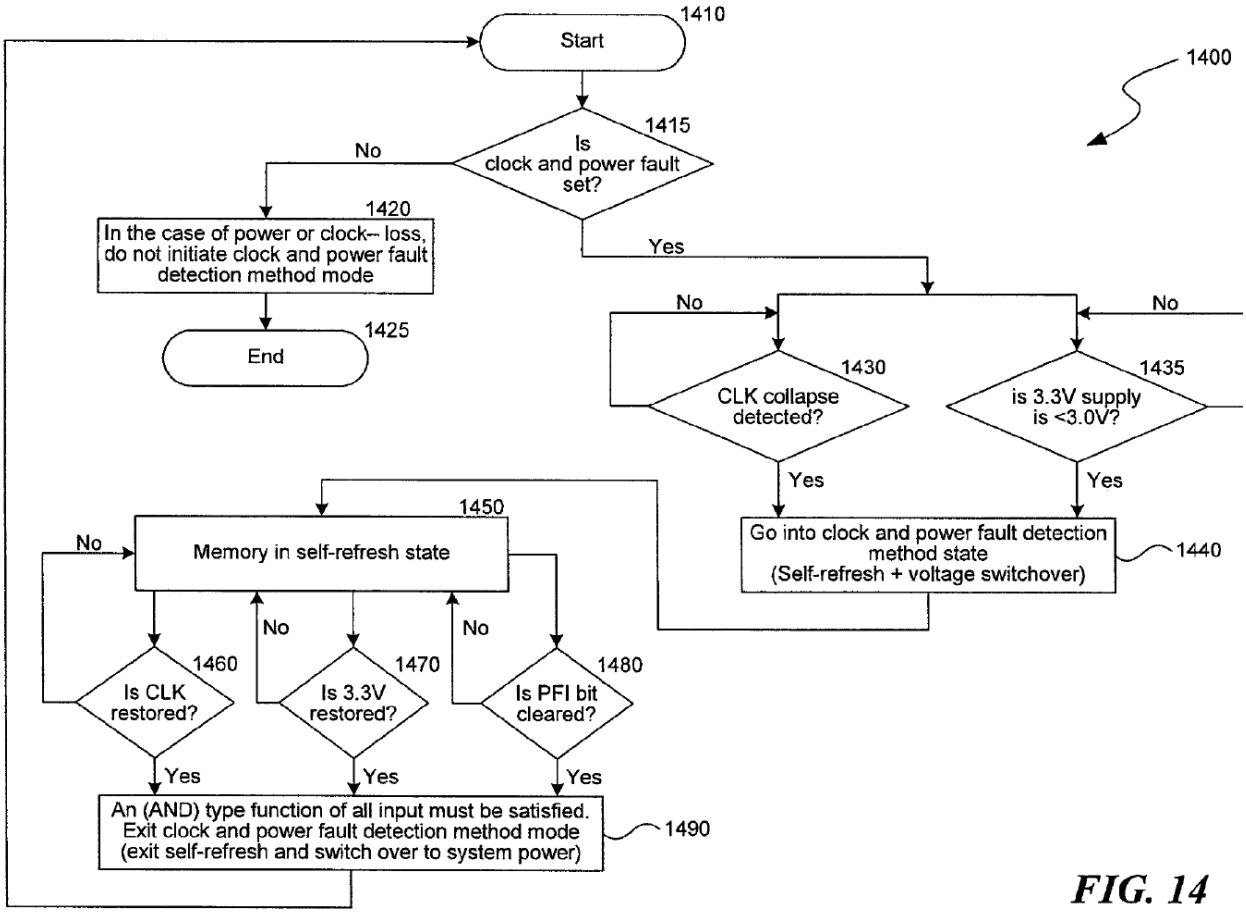


FIG. 14

Furthermore, Spiers's invention is not limited to detecting undervoltage conditions, EX1025, ¶[0041] ("power failure, power interruption, or other failure"), and thus it would have been obvious to implement Spiers's detector 202

to detect both undervoltage and overvoltage conditions, to avoid losing data or damaging the circuits. EX1003, ¶¶773-778; EX1023, ¶[0013] ("tolerance (e.g., around +/−15%) can be accommodated."). Detecting both undervoltage and overvoltage conditions was common practice and included in commercially available products, including specifically for PCI products like Spiers. EX1063, pp.1-2 (below); EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

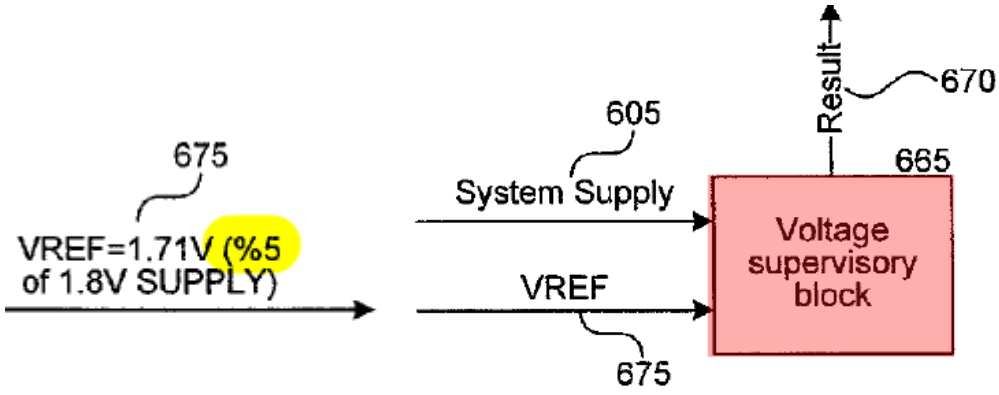
Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

7. Claim 6

As explained directly above for claim 5, Grounds 4A-4C also teach undervoltage protection, as required by claim 6: "*claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to*

the power input voltage having a voltage amplitude that is less than a second threshold voltage." EX1003, ¶¶781-787; EX1024, 4:44-52, 5:35-43, 8:23-29, 9:8-12, Figs. 5, 6 (675, below, showing a threshold of -5% to detect voltage anomalies), 8, 14-15.



8. Claim 7

Grounds 4A-4C teach "*claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage* [e.g., +5V, EX1025, ¶[0037]]." EX1003, ¶¶790-798. As discussed for claims 5-6, Grounds 4A-4C teach the "*second threshold voltage*" corresponds to an undervoltage tolerance the module can safely handle. EX1003, ¶¶764-789. Amidi (part of the combination for Ground 4) teaches undervoltage detection at 5% and 10% below nominal. EX1024, Fig. 6 (VREF, 675, 5% below nominal, above), 8:23-36, Fig. 14 (10% below nominal, second figure below). More generally, a range of +/-10% or +/-15% for undervoltage and overvoltage detection was common, and thus any threshold within that range would be obvious under Federal

Circuit precedent discussed above (p.27). *See, e.g.*, EX1023, ¶[0013] (+/-15%); EX1063, pp.1-2 (+/- 10%, reproduced below); EX1024, 8:23-36, Fig. 14 (reproduced below); EX1027, p.32 (VDDSPD is 3.3V +/-10%); EX1061, p.15 (programmable under- and over-voltage protection over a range, including 10%).

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PCI Local Bus Power Supervisor

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

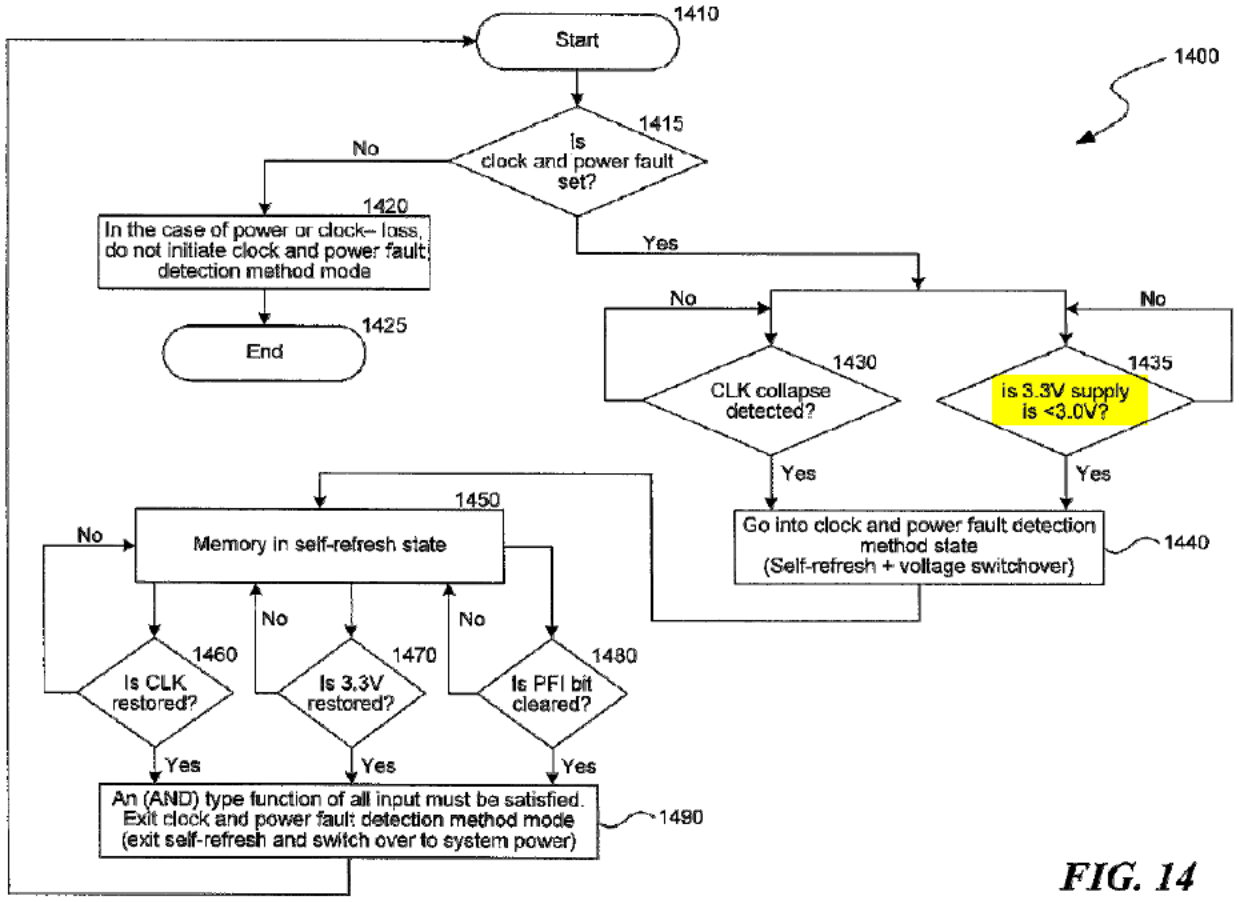


FIG. 14

9. Claim 8

a) [8.a] Preamble and [8.b] One or More Registers [8.b.1] Coupled to one of the regulated voltages and [8.b.2] configured to register address and control signals

Grounds 4A-4C teach "*claim 1, the plurality of components further comprising: one or more registers* [e.g., in Spiers' processor 198, to capture received PCI signals and to translate those to signals usable by the SDRAMs] *coupled to one of the first, second, third and fourth* [e.g., V_{CCO} for the processor's PCI interface, as discussed above (pp.78-81, 87)] *regulated voltages, the one or more registers configured to register, in response to a clock* [e.g., bus clock (CLK)

below], *the first plurality of address and control signals* [from [1.b] and [1.i.2], e.g., on lines AD and C/BE, respectively, below]." EX1003, ¶¶799-813. This is illustrated in the PCI specification (further below), which a POSITA would have understood to explain the functioning of Spiers' PCI bus. EX1025, Fig.9 (annotated below), ¶¶[0037, 44-46]; EX1031, pp.7, 47-48 (further below, showing PCI read and write operations with address (AD), command (C/BE), and data (AD) signals transmitted in sync with the bus clock (CLK)).

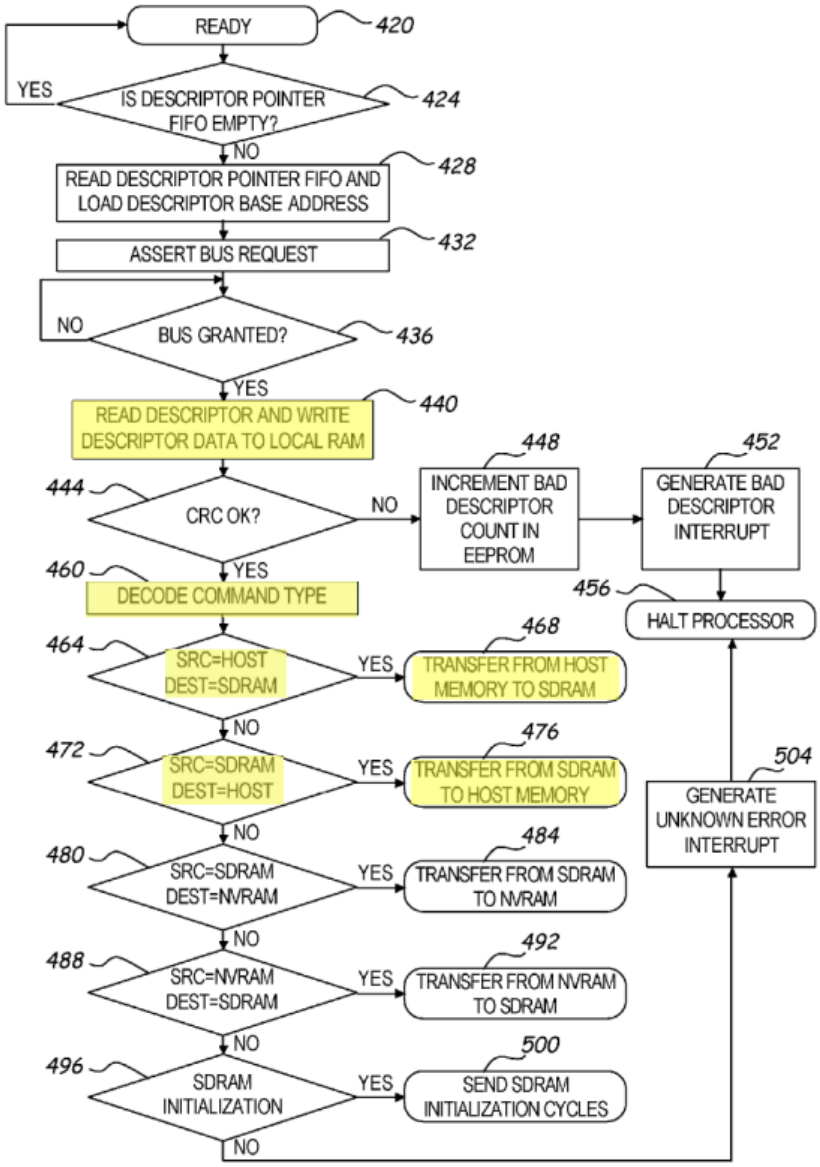

READY
420
YES
IS DESCRIPTOR POINTER FIFO EMPTY?
424
NO
READ DESCRIPTOR POINTER FIFO AND LOAD DESCRIPTOR BASE ADDRESS
428
ASSERT BUS REQUEST
432
NO
BUS GRANTED?
436
YES
READ DESCRIPTOR AND WRITE DESCRIPTOR DATA TO LOCAL RAM
440
444
CRC OK?
NO
448
INCREMENT BAD DESCRIPTOR COUNT IN EEPROM
452
GENERATE BAD DESCRIPTOR INTERRUPT
YES
460
DECODE COMMAND TYPE
456
HALT PROCESSOR
464
SRC=HOST DEST=SDRAM
YES
468
TRANSFER FROM HOST MEMORY TO SDRAM
NO
472
SRC=SDRAM DEST=HOST
YES
476
TRANSFER FROM SDRAM TO HOST MEMORY
504
GENERATE UNKNOWN ERROR INTERRUPT
NO
480
SRC=SDRAM DEST=NVRAM
YES
484
TRANSFER FROM SDRAM TO NVRAM
NO
488
SRC=NVRAM DEST=SDRAM
YES
492
TRANSFER FROM NVRAM TO SDRAM
NO
496
SDRAM INITIALIZATION
YES
500
SEND SDRAM INITIALIZATION CYCLES
NO

FIG.9

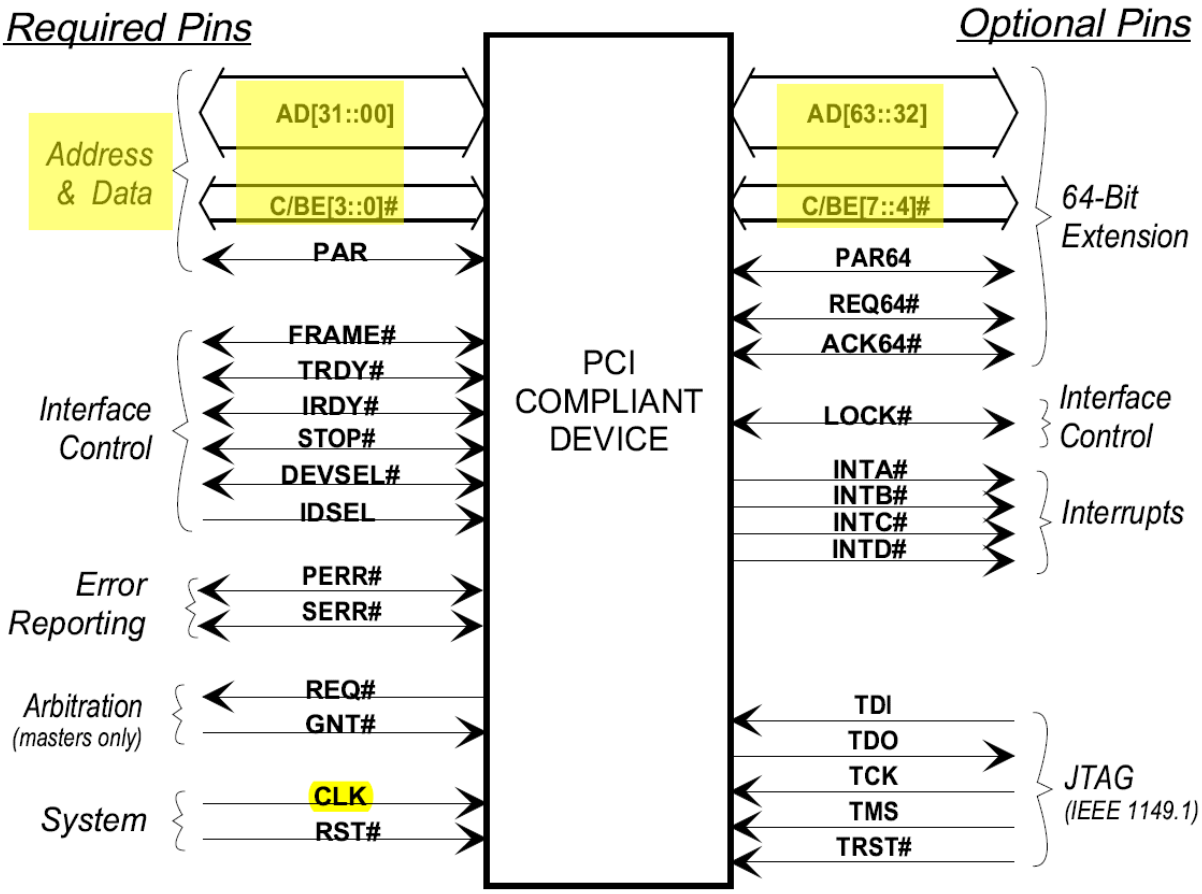


Figure 2-1: PCI Pin List

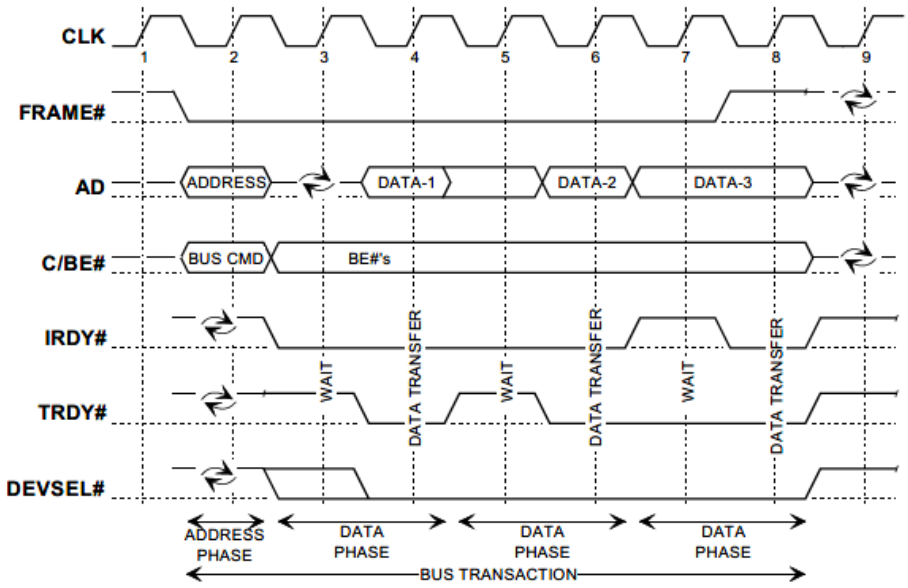


Figure 3-5: Basic Read Operation

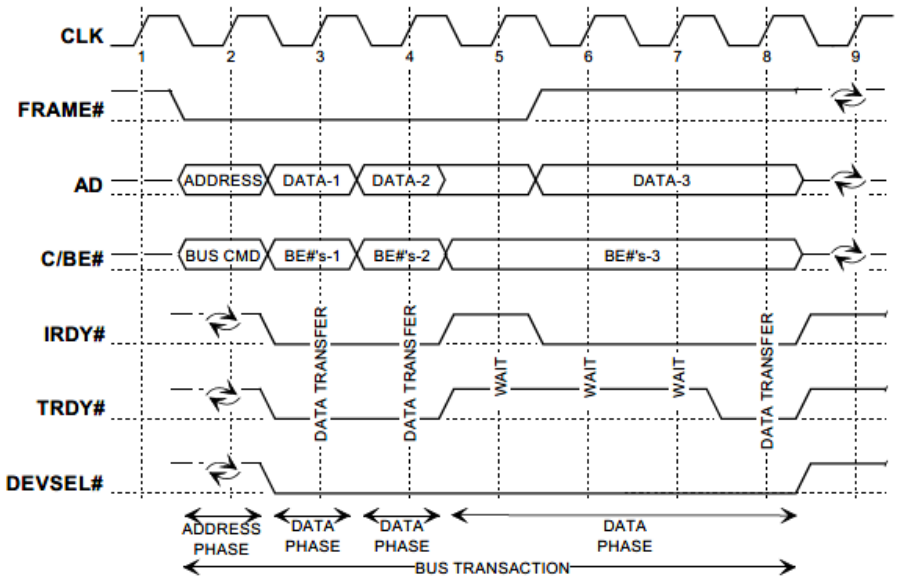
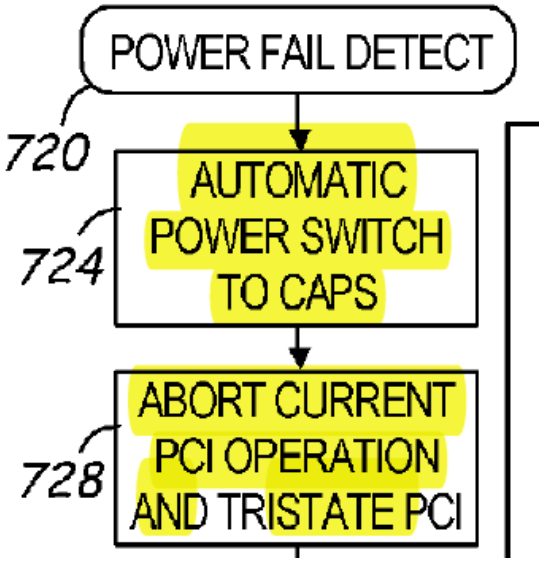


Figure 3-6: Basic Write Operation

b) [8.b.3] Wherein one of the voltages is selectively switched off

Grounds 4A-4C teach "*wherein the one of the first, second, third and fourth regulated voltages* [e.g., V_{CCO} to the processor's PCI interface, see [8.b.1]] *is selectively switched off to turn power off to the one or more registers* [e.g., to conserve power during S3 sleep mode (where the SDRAMs are in self-refresh mode and power to the processor is turned off), or, in the case of power failure, because Spiers' processor "aborts any current PCI operation and tristates the PCI" (728 below) so power to the PCI interface and the corresponding logic can be switched off] *while one or more components of the plurality of components are powered on* [e.g., capacitors power the backup device 144 while moving data from volatile to non-volatile memory during the power failure]." EX1003, ¶¶814-825; EX1025, ¶¶[0034, 36-37, 54-56], Fig.14 (below in part and in whole).


POWER FAIL DETECT
720
AUTOMATIC POWER SWITCH TO CAPS
724
ABORT CURRENT PCI OPERATION AND TRISTATE PCI
728

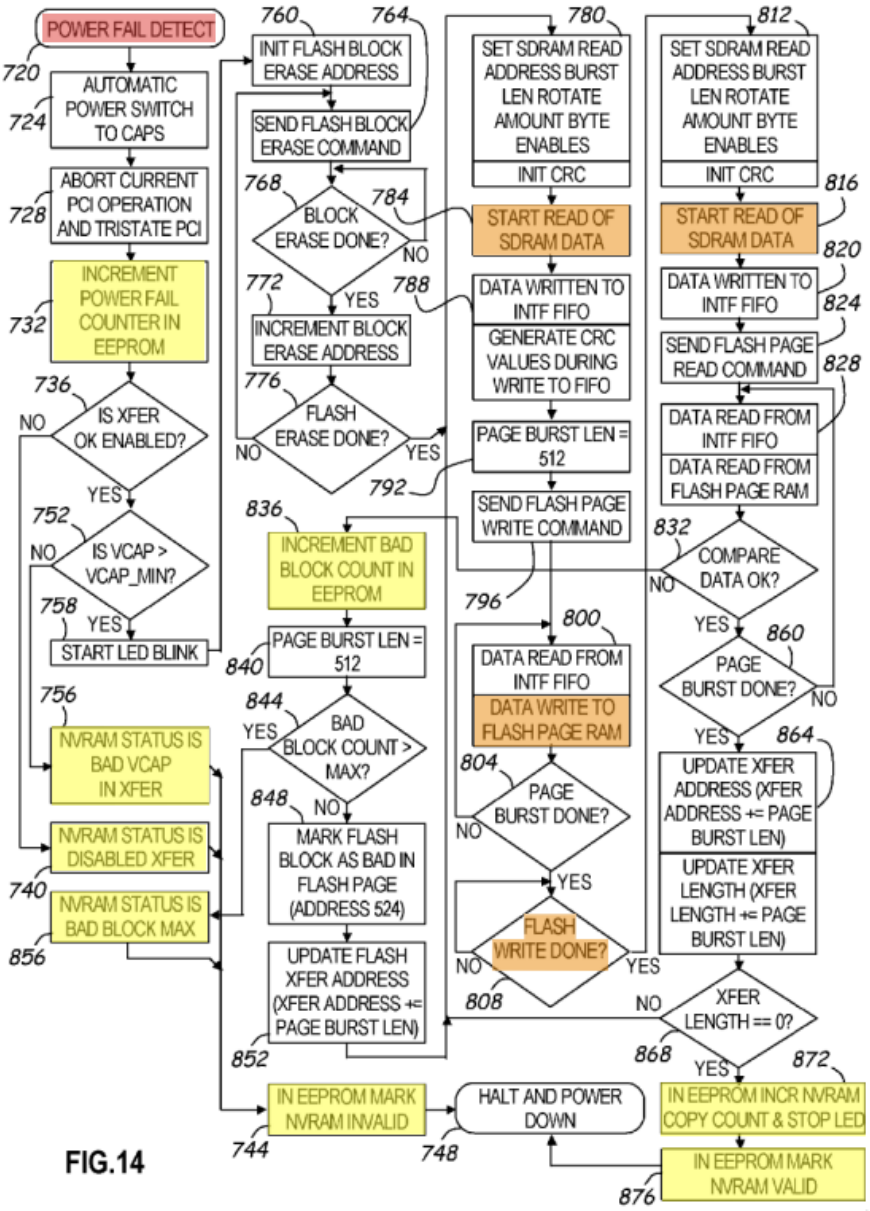


FIG.14

Switching off power to an interface which is not in use was a well-known power-saving technique at the time. EX1033, 9:57-60, 12:50-58. For example, Amidi discloses disconnecting the system bus when using backup power. EX1024, Fig.12 (annotated below), 7:35-43. Power to the interface is also turned off in the well-known S3 mode while the memories are in self-refresh mode. EX1027, pp.21

("1.5V, Vtt, and 3.3V are off"), 39; EX1039, ¶[0065]. Power to the "*registers*" could be turned off either by turning off the relevant buck converter (to save maximum power) or with a switch to selectively allow/prevent V_{CCO} from reaching the "*registers*" (to avoid any delays with restarting the buck converter when power is turned back on). EX1003, ¶¶817-818; EX1056, Abstract, 3:5-11, 5:15-26 ("switch"), Fig.3.

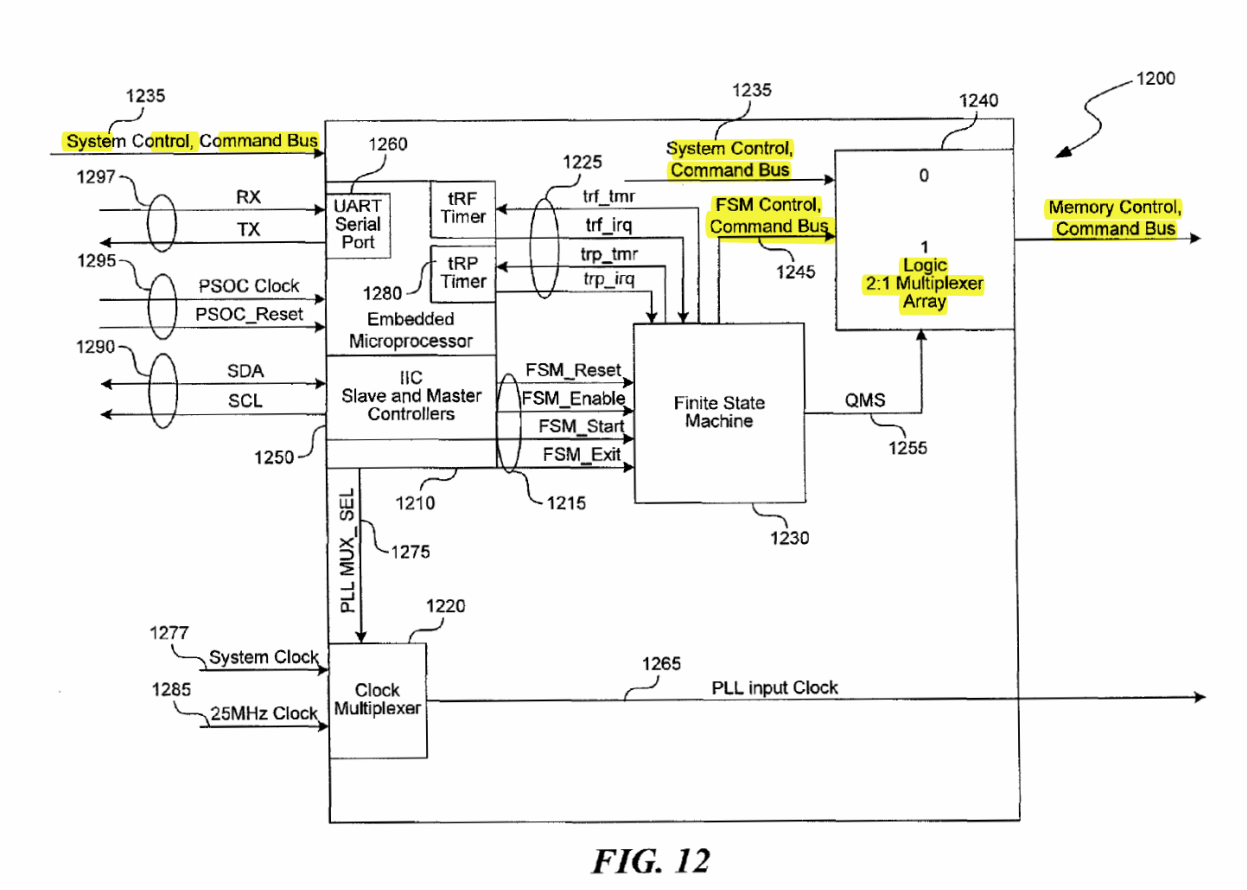


FIG. 12

10. Claim 9

As explained for claims 5 to 7 above (pp.102-108), Grounds 4A-4C also teach overvoltage protection with a 10% threshold, as required by claim 9: "*claim*

5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage." EX1003, ¶¶826-831.

11. Claim 10

Grounds 4A-4C teach "*claim 5, the plurality of components further comprising: a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information*." EX1003, ¶¶832-839. Spiers teaches that its module includes "*a logic element*," including part of the processor 198, and non-volatile memories EEPROM 210 and NAND Flash memory 194, implementing the process of Figure 14. EX1025, ¶¶[0038, 54-56], Fig.14 (below).

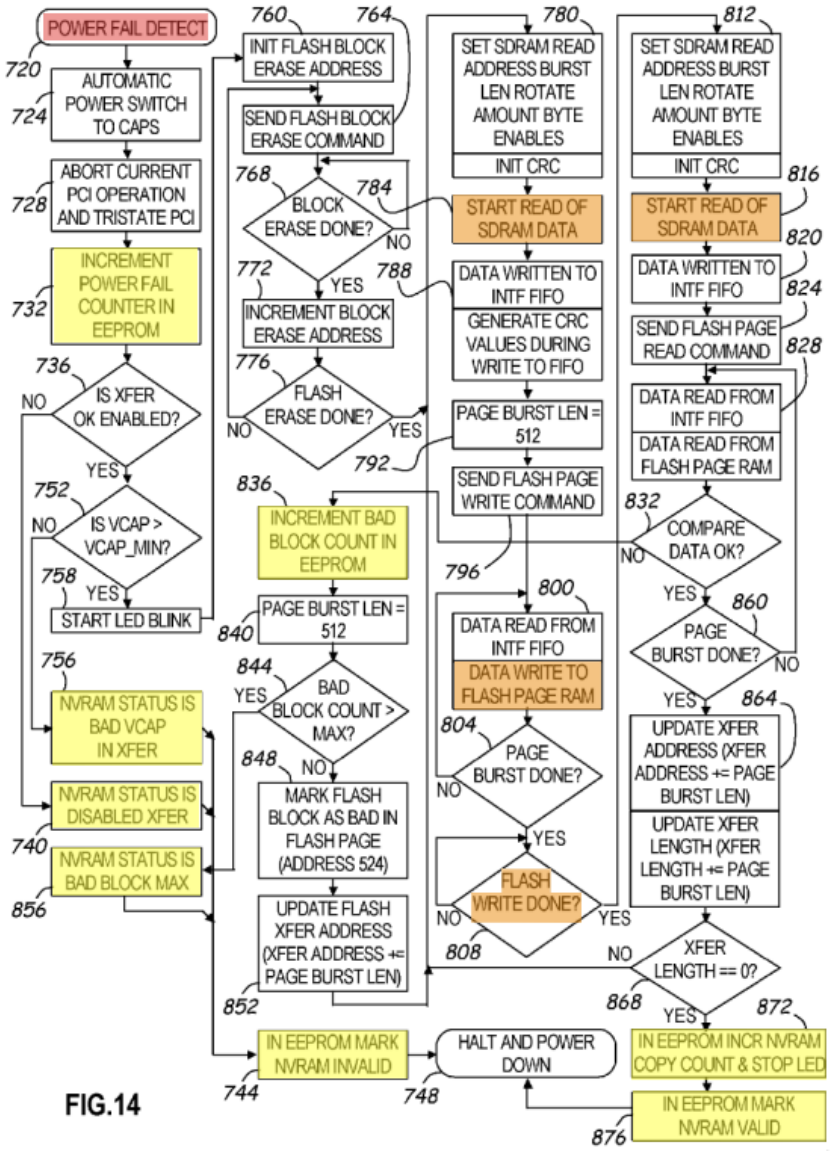


FIG.14

Yellow annotations above indicate examples of storing information in a non-volatile memory EEPROM 210, including "*configuration information,*" such as status indicators. EX1003, ¶¶838, 824.

12. Claim 11

Grounds 4A-4C teach "*claim 10, wherein, in response to the trigger signal* [from claim 5], *the logic element writes information into the non-volatile memory*."

EX1003, ¶¶840-844. Spiers teaches that, when "*the logic element*" (including part of processor 198) receives an indication of power failure ("*the trigger signal*," step 720 (red)), it writes status information into EEPROM 210 and user data from the SDRAM devices into NAND Flash memory 194 (orange). EX1025, ¶¶[0038, 54-56], Fig. 14 (below).

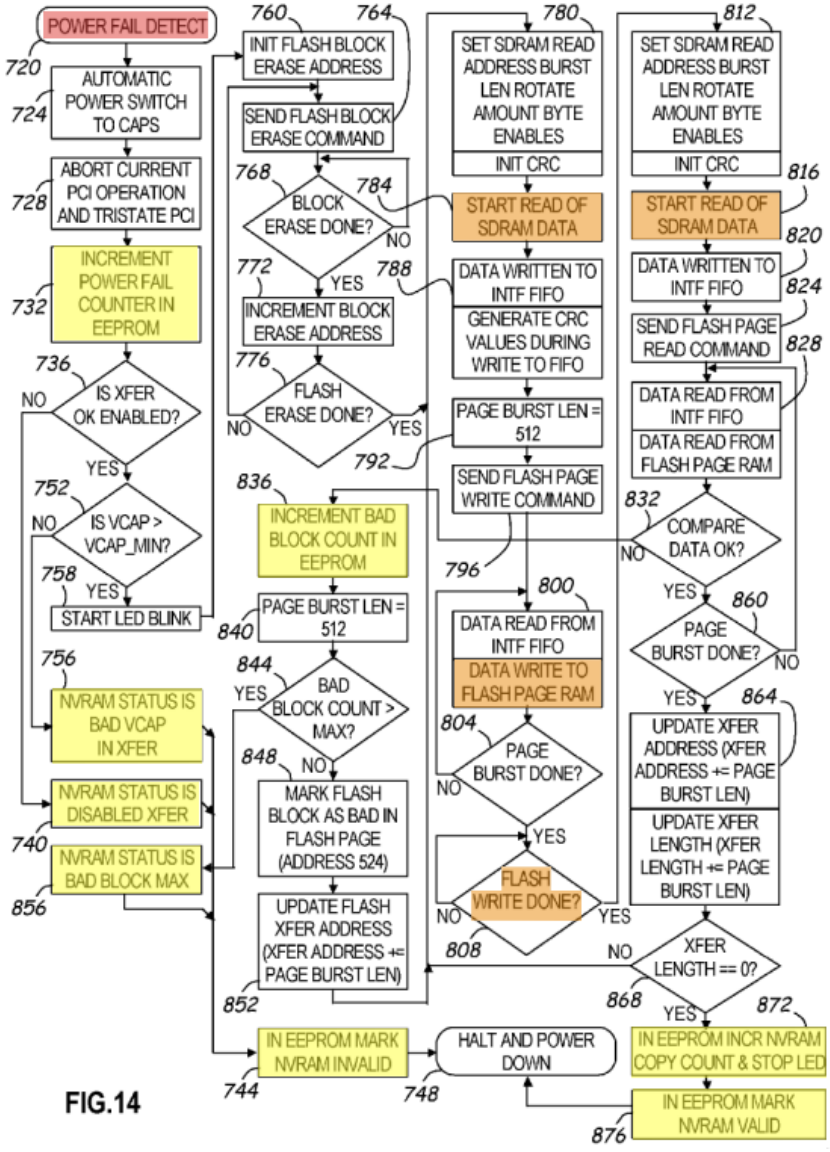


FIG.14

13. Claim 12

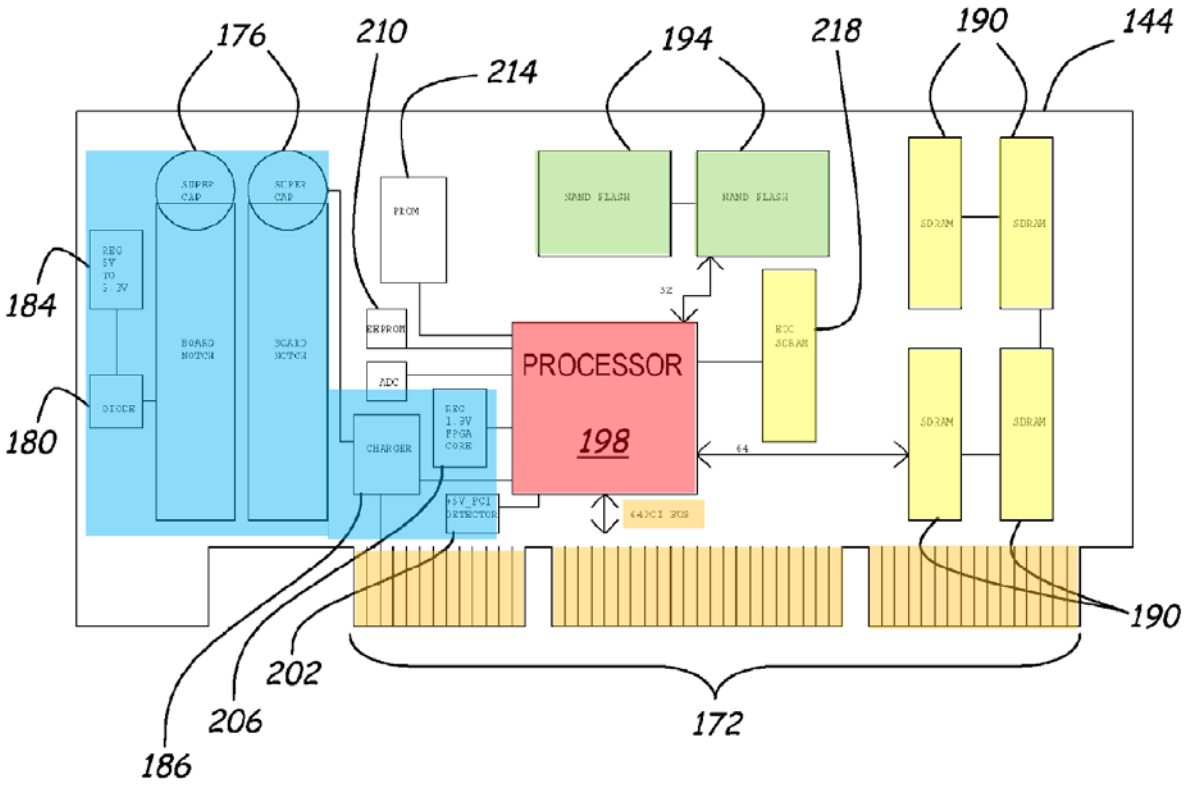
a) [12.a] Preamble and [12.b] A Non-Volatile Memory

As discussed above for claims 10 and 11 (pp.116-118), Grounds 4A-4C teach "*claim 5, the plurality of components further comprising: a non-volatile memory….*" EX1003, ¶¶845-854.

b) [12.c] A Controller

Under Netlist's apparent interpretation, where storing configuration data is a "*write operation,*" Grounds 4A-4C teach "*a controller* [e.g. in Spiers's processor] *configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory,*" for the reasons discussed above for claims 10 and 11 (pp.116-118). EX1003, ¶¶856, 836-844.

Grounds 4A-4C also teach this limitation under a narrower interpretation requiring writing user data from volatile to non-volatile memory: Spiers's processor 198 (red, below) includes "*a controller*" that receives the trigger signal (e.g., at step 720 of Fig.14, "Power Fail Detect"), and in response, "mov[es] data from the volatile memory [yellow] to the non-volatile memory [green]," EX1025, ¶[0037], thus "*perform[ing] a write operation to the non-volatile memory*." EX1003, ¶¶857-859; EX1025, Fig. 5 (below), ¶[0037] (disclosing multiple SDRAMs (190, yellow) and NAND flash modules (194, green)), [0054-56], Fig. 14 (above, providing process for writing user data to non-volatile memory).



14. Claim 13

Grounds 4A-4C teach "*[t]he memory module of claim 5, wherein the power input voltage* [of +5V PCI] *is coupled to the first, second, and third buck converters and the converter circuit*" for the reasons discussed above with reference to claim elements [1.c]-[1.f] when the power input voltage is in the normal operating range as discussed for claim 5 (e.g., no power failure detected). EX1003, ¶¶860-864.

15. Claim 14

Grounds 4A-4C teach "*[t]he memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers* [e.g., following the restoration of

power after power failure, as illustrated in Spiers' Fig.8 (below)], *the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices* [e.g., as discussed in [1.i.2] and [8.b.2] for normal operation]." EX1003, ¶¶865-869; EX1025, ¶¶[0041, 43], Fig.8.

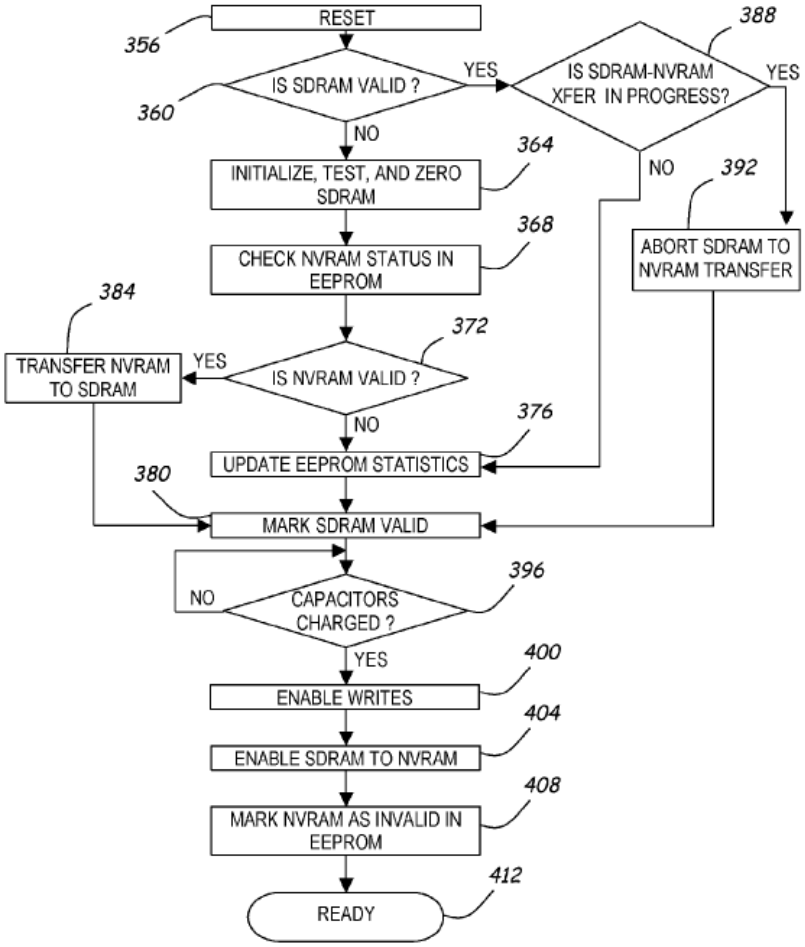
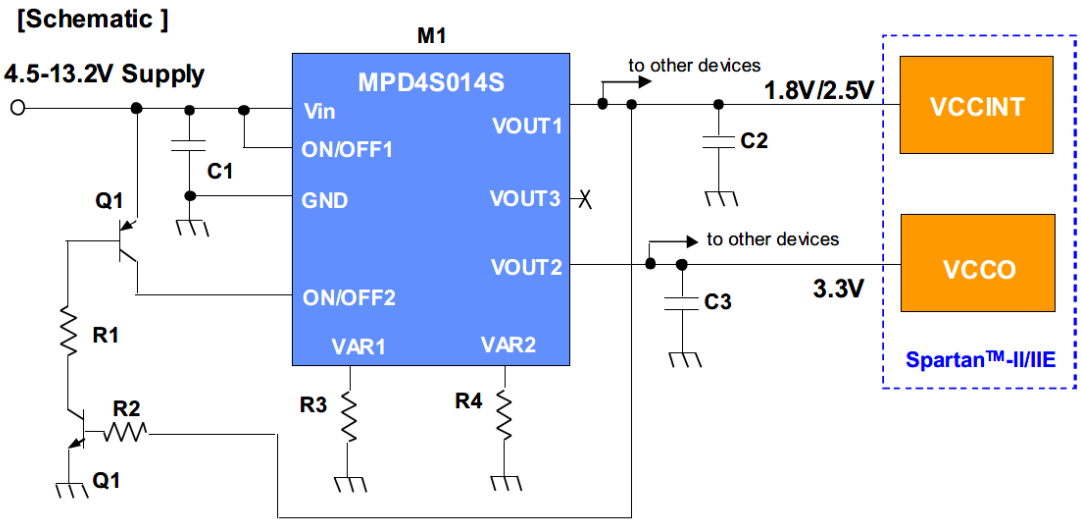


FIG.8

16. Claim 15

Grounds 4A-4C teach "*[t]he memory module of claim 1, the plurality of components further comprising: a logic element including one or more integrated*

circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information." EX1003, ¶¶870-879. As discussed for claim 10 above (pp.116-117), Spiers teaches that its module includes "*a logic element*" implementing the process of Figure 14, including "*one or more integrated circuits*" such as parts of the FPGA processor 198 and non-volatile memories EEPROM 210, where EEPROM 210 is "*configured to store configuration information*," such as status indicators. It would be obvious to a POSITA that the FPGA processor 198 ("*logic element*") also includes "*discrete electrical elements*," such as resistors and capacitors as required for interconnections and settings for the FPGA processor. *See, e.g.*, EX1042, p.16 (below); EX1028, p.13 (similar for AMB Buffer).



To the extent "*an internal non-volatile memory*" is satisfied by an integrated circuit that includes non-volatile memory and an interface, Spiers's EEPROM 210 discloses that. EX1025, ¶[0038]. To the extent "*an internal non-volatile memory*" requires integration with the FPGA processor 198 of Spiers, it would have been obvious to a POSITA, because such FPGA's were commercially available. EX1003, ¶878; EX1025, ¶[0037] ("FPGA"); EX1067, p.1-1 (FPGA with internal non-volatile memory). An FPGA with built-in non-volatile memory decreases the number of components, interfaces and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. EX1003, ¶878; EX1067, pp.1-1, -2 ("instant-on," "secur[e]"); EX1066, 26:64-27:4 (teaching configuration information may be "stored in a … register on the buffer or controller device").

17. Claims 16-30

Claims 16 and 30 add a new limitation, "*pre-regulated input voltage*," discussed below (pp.126-127), but otherwise Grounds 4A-4C disclose claims 16-19, 21-28, and 30, and Grounds 4B-4C disclose claims 20 and 29 (requiring 1.8V to the SDRAM), for at least the same reasons discussed above, because these claims have limitations substantially identical to earlier limitations, as shown in the following table:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[16.a]	[1.a]	¶¶881-884 (¶¶641-646)
[16.b]	[1.b]	¶¶885-888 (¶¶647-654)
[16.c]	[1.c]-[1.e][10]	¶¶889-895 (¶¶655-688)
[16.d.1]	[1.f], [16.c]	¶¶896-899 (¶¶689-700, 889-895)
[16.d.2]	[1.c]-[1.f]	¶¶900-903 (¶¶655-700)
[16.e]	[1.g]-[1.h]	¶¶904-907 (¶¶701-718)
[16.f]	[5.a]-[5.b][11]	¶¶908-912 (¶¶764-780)
[17]	[2][12]	¶¶913-922 (¶¶739-746)
[18.a]	[16.a]	¶¶924-926 (¶¶881-884)
[18.b]	[12.c]	¶¶927-930 (¶¶855-859)
[19]	[12.c]	¶¶931-935 (¶¶855-859)
[20]	[1.h], [3]	¶¶936-940 (¶¶714-718, 747-751)
[21.a]	[16.a]	¶¶942-944 (¶¶881-884)
[21.b.1]	[1.i.1]	¶¶945-948 (¶¶719-723)

[10] With respect to "*pre-regulated input voltage*" in [16.c], see pp.126-127.

[11] See note 5 on p.71.

[12] See note 6 on p.71. EX1003, ¶¶913-922.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[21.b.2]	[1.i.2][13]	¶¶949-952 (¶¶724-729)
[21.b.3]	[1.i.3]	¶¶953-956 (¶¶730-734)
[21.b.4]	[1.i.4]	¶¶957-960 (¶¶735-738)
[22.a]	[16.a]	¶¶962-964 (¶¶881-884)
[22.b]	[10.b], [15.b][14]	¶¶965-968 (¶¶836-839, 874-879)
[23.a]	[1.a]	¶¶970-973 (¶¶641-646)
[23.b]	[1.b]	¶¶974-977 (¶¶647-654)
[23.c.1]	[1.g]	¶¶978-981 (¶¶701-713)
[23.c.2]	[1.h], [1.i.1], [1.i.3], [8.b.1]	¶¶982-985 (¶¶714-723, 730-734, 803-809)
[23.c.3]	[1.i.2], [8.b.2]	¶¶986-989 (¶¶724-729, 810-813)
[23.d]	[1.c]-[1.e]	¶¶990-993 (¶¶655-688)
[23.e]	[1.f]	¶¶994-997 (¶¶689-700)
[23.f]	[8.b.3], [14]	¶¶998-1001 (¶¶814-825, 865-869)

[13] See note 7 on p.72.

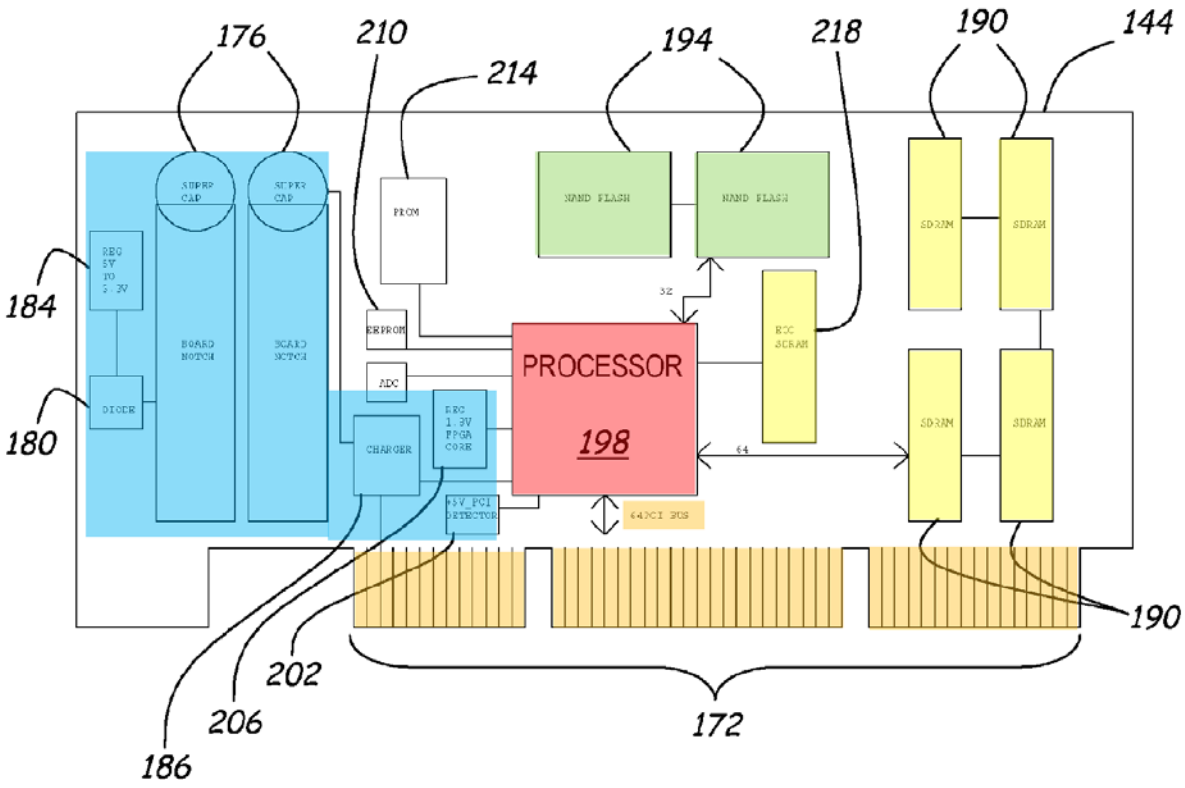
[14] In [22.b], "*the configuration information* [e.g., status indicators stored in the non-volatile memory in the logic element as discussed in [10.b] and [15.b]] *is used to program the logic element* [e.g., to transfer data to non-volatile memory during a power disruption]." EX1003, ¶¶824, 968; EX1025, ¶¶[0054-56], Fig.14.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[23.g]	[14]	¶¶1002-1005 (¶¶865-869)
[23.h]	[8.b.3][15]	¶¶1006-1009 (¶¶814-825)
[24.a]	[23.a]	¶¶1011-1013 (¶¶970-973)
[24.b]	[5.b]	¶¶1014-1017 (¶¶767-780)
[25.a]	[24.a]	¶¶1019-1021 (¶¶1011-1013)
[25.b]	[12.c]	¶¶1022-1025 (¶¶855-859)
[26]	[12.c]	¶¶1026-1030 (¶¶855-859)
[27]	[6]	¶¶1031-1035 (¶¶781-789)
[28]	[17]	¶¶1036-1040 (¶¶913-922)
[29]	[20]	¶¶1041-1045 (¶¶936-940)
[30]	[1.c]-[1.f], [13], [16.c]-[16.d.1]	¶¶1046-1050 (¶¶655-700, 860-864, 889-899)

For [16.c] and 30, to the extent a "*pre-regulated input voltage*" can be satisfied by the "*input voltage*" of [16.f] being within pre-determined limits, as suggested by Netlist, EX1071, p.43; EX1073, pp.49-50, Spiers teaches that by disclosing a PCI connector, EX1025, ¶[0037], which was standardized to receive a "5V" "Supply Voltage" with a +/- 0.25V tolerance, EX1031, p.117; EX1003, ¶893.

[15] See note 3 on p.51. EX1003, ¶1009.

To the extent the "*pre-regulated input voltage*" must be a voltage pre-regulated on the memory board itself, EX1001, 28:53-58, Spiers teaches that with "voltage ***regulator*** 184," which is connected to the capacitors 176 and used during "power failure," *see* EX1025, ¶[0037], Fig.5 (below); EX1003, ¶894. Furthermore, it would have been obvious to pre-regulate the system power from 5V down to 3.3V (similar to voltage regulator 184) to provide further stability and to allow using the same voltage converters for powering the components both during normal operation with system power and with the capacitors during a power failure. *Id.*



E. Ground 5

Ground 5 renders obvious claims 1-30.

1. Ground 5 combination: Ground 4 + Hajeck (EX1038)

Ground 5 combines Ground 4 with the teachings of Hajeck, which teaches a "voltage detection circuit 48" for detecting both undervoltage and overvoltage anomalies in memory subsystems. EX1038, 3:30-40, Fig.1; EX1003, ¶¶207-212. Hajeck is analogous art to Spiers and Amidi in Ground 4 as all relate to memory modules in general and protecting against power disruptions in particular. EX1003, ¶208. A POSITA would have been motivated to combine Ground 4 with the teachings of Hajeck, and had a reasonable expectation of success in doing so, because Spiers discloses a +5V PCI detector 202 to detect voltage anomalies and to switch to backup power, EX1025, ¶¶[0002, 37, 54], similar to Amidi, EX1024, 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs.5-6, 14-15, and Hajeck teaches the importance of detecting both undervoltage and overvoltage conditions to avoid data loss, EX1038, 1:10-31, 3:30-40, 4:62-65, consistent with voltage detection circuits for PCI cards (like Spiers) that were readily available at the time:

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5; EX1061, p.15; EX1062, p.15.

The teachings of Hajeck do not affect any of the voltage mappings in Ground 4, and thus the voltage mappings for Grounds 5A-5C are the same as those for Grounds 4A-4C above (pp.87, 78-81).

2. Claims 1-30

Ground 5 renders obvious claims 1-30 for at least the same reasons provided above for Ground 4 (pp.82-127). To the extent one were to argue that Ground 4 fails to teach overvoltage protection as required by [5.b] and discussed above (pp.102-105) — and also required by claims 6-7, 9-13, [16.f], 17-22, 24-27 — such overvoltage protection was obvious in light of Hajeck in the combination for Ground 5 discussed above (pp.128-129). EX1003, ¶¶779-780. In particular, in the

combination of Ground 5, Spiers's "+5V PCI detector 202" would be implemented to detect voltage anomalies and switch to the backup power not only for undervoltage conditions as taught by Spiers and Amidi, EX1025, ¶¶[0002, 36-37], Fig.14; EX1024, 4:44-53, but also "when the voltage exceeds a certain level" as taught by Hajeck, EX1038, 3:30-43; *see also id.* Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, Fig. 1. Thus, Ground 5 further teaches both overvoltage and undervoltage detection and protection, further rendering obvious claims 5, 16, 24, and their dependents (6-7, 9-13, 17-22, and 25-27). EX1003, ¶¶779-780, 788, 830, 912, 1017.

VII. *FINTIV*

The *Fintiv* factors favor institution. There are two cases currently pending between the parties that involve the 918 Patent, but both are in their infancy. EX1068-73. There currently is no trial date in either case, nor have any discovery requests been served. This petition was filed quickly, approximately 4.5 months after Petitioner waived service of Netlist's complaint.

VIII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-30 be canceled as unpatentable.

Dated: May 17, 2022

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24 because it contains 13,997 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 17th day of May, 2022, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

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